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OPTIMAL SWITCHING SEQUENCE MODEL PREDICTIVE CONTROL FOR POWER ELECTRONICS

TESIS PARA OPTAR AL GRADO DE
DOCTOR EN INGENIERÍA ELÉCTRICA

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RESUMEN DE LA TESIS PARA OPTAR GRADO DE
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POR: ANDRÉS FELIPE MORA CASTRO
FECHA: MARZO 2019
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En este proyecto de tesis, se propone una estrategia de control predictivo (MPC, por sus siglas en inglés) basada en el concepto de secuencia de conmutación óptima (OSS) recientemente introducido para convertidores de punto neutro enclavado de tres niveles (3L-NPC) conectados a la red eléctrica.

La metodología de control propuesta, llamada OSS-MPC en cascada (C-OSS-MPC), considera explícitamente el modulador en su formulación junto con el modelo del sistema. Como se verificó a lo largo de esta tesis, la estrategia C-OSS-MPC está formulada para el control de la corriente o el control directo de la potencia activa/reactiva como variables primarias de control, mientras que el problema del equilibrio de voltaje del enlace CC se resuelve sin utilizar factores de ponderación en un bucle de control interno basado en una novedosa y sencilla estrategia de control MPC. Por lo tanto, la metodología de control propuesta controla de manera óptima tanto el objetivo de control primario como los voltajes de los condensadores de este convertidor de potencia. Bajo esta perspectiva, la dificultad de diseñar el factor de ponderación se evita en este trabajo y el rendimiento del sistema controlado no se ve afectado por un punto de operación particular del convertidor conectado a la red.

La estrategia MPC resultante permite operar el convertidor con un espectro armónico predefinido, frecuencia de conmutación fija y una respuesta dinámica rápida y robusta en todo el rango operativo del convertidor de potencia, superando las estrategias MPC existentes en la literatura para los convertidores de potencia. Además, se ha propuesto un nuevo y eficiente algoritmo de optimización para encontrar rápidamente la solución óptima con el fin de hacer posible una implementación en tiempo real de la estrategia de control propuesta.

Finalmente, se proporcionan resultados experimentales y de simulación para demostrar la efectividad y el rendimiento de alta calidad de la estrategia de control propuesta, lo que hace que este enfoque de control no solo sea adecuado para las aplicaciones de convertidor de potencia conectado a la red, sino que también para accionamientos eléctricos de alta potencia.

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In this thesis project, a model predictive control (MPC) strategy based on the recently introduced optimal switching sequence (OSS) concept is proposed for grid-connected three-level neutral-point clamped (3L-NPC) converters.

The proposed Cascaded-OSS-MPC (C-OSS-MPC) methodology explicitly considers the modulator in its formulation along with the model of the system. As verified throughout this thesis, the C-OSS-MPC strategy is formulated for either grid current or direct active/reactive power control as control primary variables, while the dc-link voltage balancing problem is addressed without utilizing weighting factors in an inner control-loop based on a novel and simple MPC strategy. Therefore, the proposed C-OSS-MPC methodology optimally controls both the primary control objective and the capacitor voltages of this power converter. Under this perspective, the difficulty of design the weighing factor is avoided in this work and the performance of the controlled system is not affected by a particular operating point of the grid-connected converter.

The resulting MPC strategy allows operating the converter with a predefined harmonic spectrum, fixed switching frequency and, a fast and robust dynamic response in the whole operating range of the power converter, outperforming existing MPC strategies for power converters. Furthermore, the author has also proposed a new and efficient optimization algorithm to promptly find the optimal solution in order to make possible a real-time implementation of the proposed control strategy.

Finally, experimental and simulation results are provided to demonstrate the effectiveness and high-quality performance of the proposed control strategy, making this control approach suitable for grid-connected power converter and high-power motor drive applications.

Dedicated to my parents Isabel and Hugo

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CHAPTER 1

Introduction

Energy has been the key in the development of the human society by helping it to control and adapt to the environment. Nowadays, from early in the morning and all day, our society requires energy to mainly produce heat, light, and motion. Because the economic activity depends on upon energy resources, its production and consumption are very important to the global economy. The energy consumption per capita in a country is thus an indicator of its state of technical development. According to [1], the energy consumption of the largest economies of Europe Union (Germany, France and the United Kingdom) represents the 51% of the total produced.

From its primary form, energy is widely available as fossil and nuclear fuels, hydro, solar, and wind energy, etc, as depicted Fig. 1.1. Nevertheless, it must be available at the point of consumption in a suitable form (thermal, mechanical electrical), at an acceptable cost and good quality, which creates problems of energy transportation from the place of origin to the final consumer considering its different physical forms. In this context, the electricity (a secondary form of energy) has been the best solution, mainly due to its flexibility, the relative efficiency of its generation and transportation stages, and finally, because it can be converted into any final form at the user level. Thereby, many applications in a wide variety of systems require of these energy conversion processes.

The fast development of the power electronics devices, along with the fast improvement of efficiency and reduction of prices on renewable energy systems, such as fuel cell, photovoltaic cells and windmills, has been changing the structure of the generation sector during the last decade. Thus, instead of incorporation of the typical huge generation power plants, several groups of small generation units, also known as Distributed Power Generation (DPG), are being incorporated to the electrical system every year [6], [7], [8]. According to The European Wind Energy Association

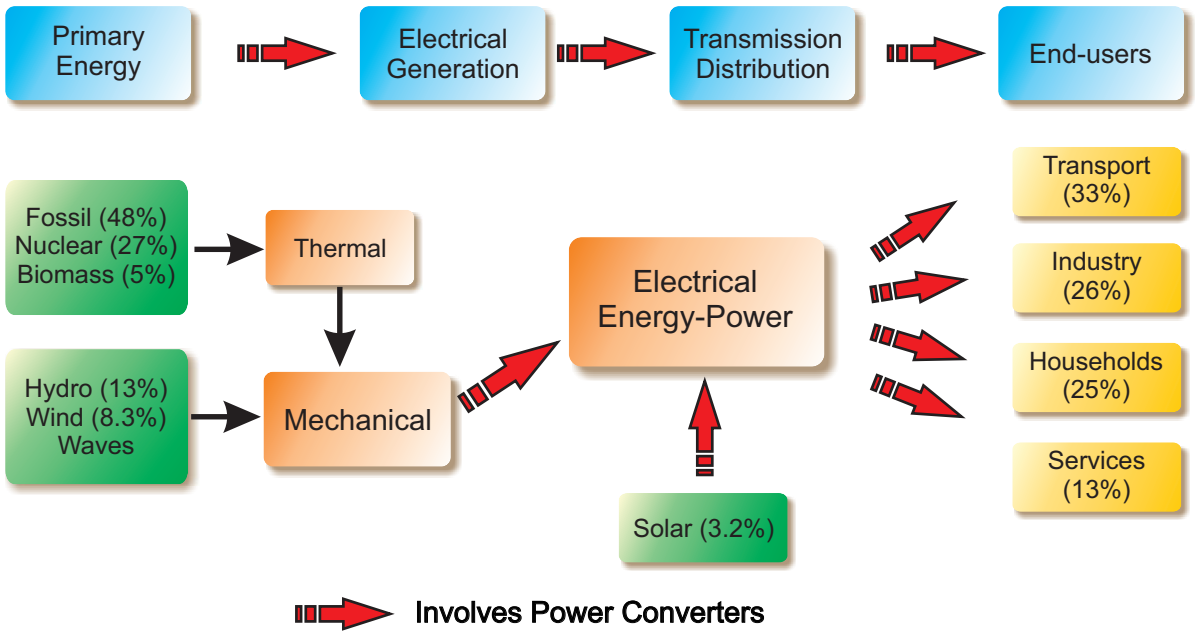

FIGURE 1.1: From primary energy to final use. Europe Union grid [1], [2] .

(EWEA) [9], the Renewable Energy System (RES) represents almost the 80% of the installed power that was incorporated in 2014.

In this context, in the last few decades, power converters and adjustable speed drives have become an enabling technology, mainly due to improved performance and higher efficiency which lead to increased production rates. Additionally, for global warming, there are a growing trend policy initiatives to focus on the integration of renewable energy resources and improving energy process efficiency in an attempt to reduce both emissions and energy demand. Considering these new requirements concerning power quality and efficiency, the conversion and control of electrical energy using power electronics is a critical topic today. To fulfil these demands new semiconductor devices, topologies, and control schemes are being developed.

1.1 The Power Converters

Since 1975, the solid-state semiconductors boosted the development of more sophisticated power electronic devices, such as IGBTs, IGCTs, GTOs, MOSFETS and Diodes [10]. By that, several high-performance applications have been introduced into the market in the last four decades, such as electrical drives for electrical machines, uninterruptible power supply, dynamic voltage restorers, active filters, static VAR compensators, dc power supplies and active front end rectifiers among others [11], [12].

From the drive applications used in industry, pumps and fans are those that account for most of the energy consumption, with power ratings up to several megawatts. The use of adjustable speed

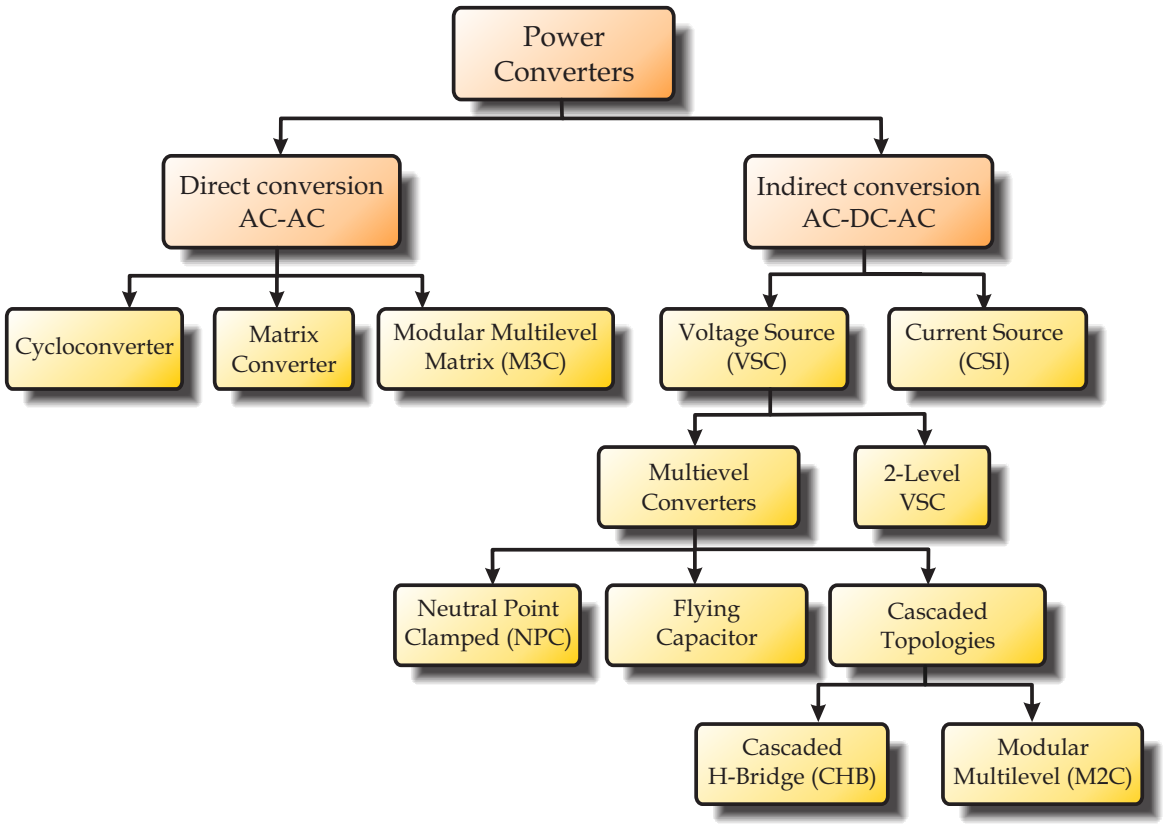

FIGURE 1.2: Power converter classification.

drives can bring significant benefits to these kinds of systems regarding performance and efficiency.

There are many types of power converters and drive systems, and every application requires different specifications that define the most appropriate topology and control scheme to be used.

A general classification of the different types of power converters is presented in Fig. 1.2, where mainly two kinds of groups are established: direct conversion AC-AC and indirect conversion AC-DC-AC. Each one of these types includes several subcategories, as depicted in Fig. 1.2. Within all available power converters in the industry, the two-level voltage source converter (2L-VSC) has become the standard topology for most of the low voltage applications such as electrical drives, and grid-connected converters. Nevertheless, in the last decades, multilevel converters have emerged as an important technology because they offer high power levels and good quality waveforms, which is clearly beneficial to the operation and control of the electrical loads [13]. One of the most popular multilevel topologies is the three-level neutral point clamped (3L-NPC) voltage source converter. This converter was introduced as a solution for medium voltage range [14] and has been extensively used in high power energy conversion systems in back-to-back configuration [15]. Another popular multilevel topology is the Cascaded H-Bridge (CHB) converter [16] mainly due to both its contribution of high power and its modularity.

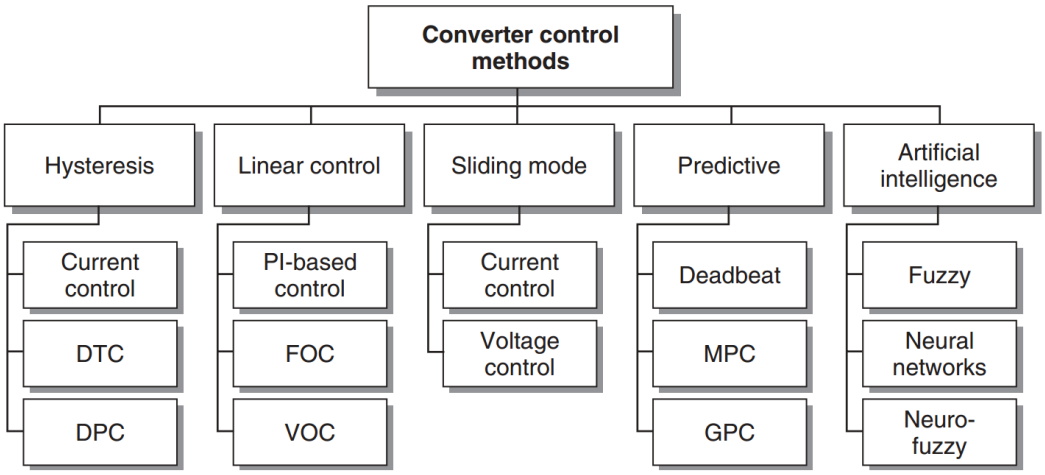

FIGURE 1.3: Control schemes for power converters and drives [3].

1.2 Control of Power Converters

Control schemes for power converters and drives have constantly been evolving according to the development of new semiconductor devices and the introduction of new control platforms. Nowadays several control methods have been proposed for converters and drives, the most commonly used ones being shown in Fig. 1.3.

1.2.1 Traditional Control Schemes

In standard approaches, the power converter is considered as the actuator which applies the required voltage given by the controller. However, due to its nature, power converters can provide only a finite number of voltage levels. For this reason, a modulation stage to synthesize the required converter output voltage is normally included. The most common modulation stage is the so-called pulse width modulation (PWM) technique [17], [18]. Here, the controller provides a modulation index, which is used by the modulator to handle the duty-cycles of the converter switches, and thus, to establish an average value of the required voltage within a sampling period. However, the obtained final switched waveform presents a harmonic spectrum, where undesired harmonic distortion appears due to the switching.

The main advantage of using a modulation stage is that the control target is decoupled of the manipulation of the converter switches. Here, it can be assumed that the power converter can provide any voltage inside a range $[v_{\min}, v_{\max}]$. Therefore, any control technique capable of dealing with bounded inputs can be implemented, within which the most popular being the proportional-integral (PI) controller with anti-windup schemes. Regarding to control method for electrical drives, the most popular scheme based on linear controllers is the field oriented control (FOC) [11], [19], where two nested control loops are used to regulate the machine speed, as is depicted in the Fig. 1.4.

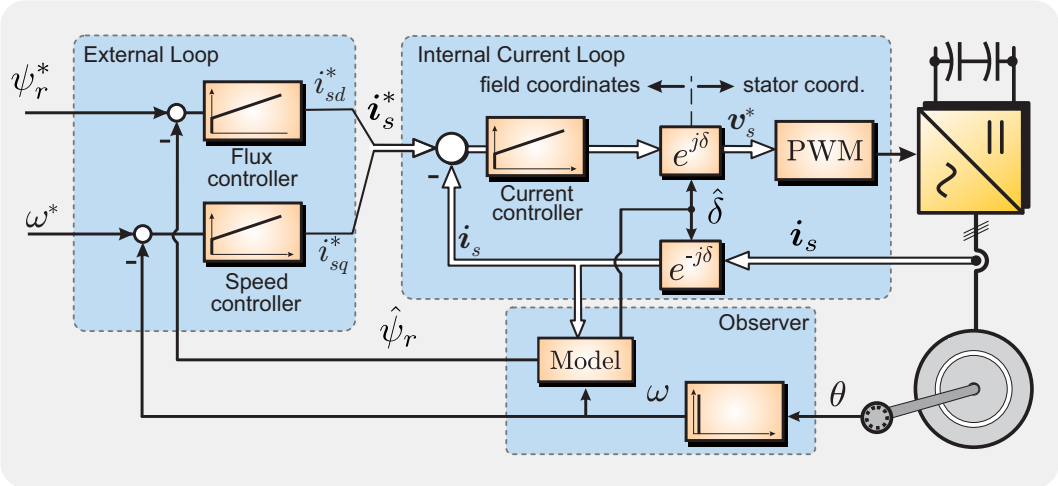

FIGURE 1.4: Fiel Oriented Control scheme

Similar concepts can be also applied for current control of grid-connected converters with voltage-oriented control (VOC) [20].

On the other hand, control techniques with implicit modulator have proposed for some applications. In these cases, the switching of the converter is not related to following a given modulation index but is determined to reduce the error of the controller goal directly. Hence, the switching states of the power semiconductors are determined by comparison of the measured variable to its reference, considering a given hysteresis band for the error [21]. Hysteresis control technique is the simplest implementation of a closed-loop control [18]. Direct torque control (DTC) for motor-drive applications [22], and its dual method for grid-connected converters, namely direct power control (DPC) [23], are the most commonly hysteresis-based control used in academia and industry.

With the development of more powerful microprocessors, new control schemes have been proposed to handle power converters. Some of the most important ones are fuzzy logic control, neural networks, sliding mode control, passivity-based control, and model predictive control [24], [25], [26], [27] and [21]. Among these new control schemes, model predictive control (MPC) is a very attractive solution for controlling power electronic converters.

1.3 State of Art of Model Predictive Control

MPC or Receding Horizon Control (RHC) is a control technique that calculates the control action by solving, at each sampling period, an optimal control problem over a finite horizon [21], [28]. To do this, RHC uses the dynamic model of the system to predictive the future system behavior from the current system state which generates an optimal control sequence. The control action to be applied to the plant is the first element of this sequence. One advantage of MPC is that concepts

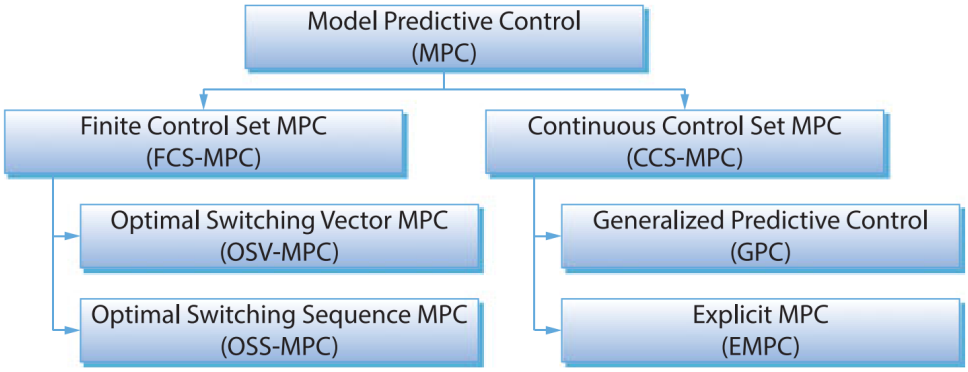

FIGURE 1.5: Classification of MPC strategies applied to power converters and drives [4].

are straightforward and intuitive and both constraints and non-linearities can be directly included at the controller formulation stage.

In the context of power electronics and electrical drives, it is convenient to classify MPC methods depending on how the switching devices are controlled and consequently, the type of optimization problem stated for computing the optimal control actions [29] [30]. As depicted in Fig. 1.5, the MPC methods are classified into two major categories.

On one hand, continuous control set MPC (CCS-MPC) computes a continuous control signal and then uses a modulator to generate the desired output voltage in the power converter. On the other hand, finite control set MPC (FCS-MPC) takes into account the discrete nature of the power converter to formulate the optimization problem and does not require an external modulator. More details regarding this MPC strategies are provided in the following.

1.3.1 Continuous Control Set MPC

If a modulator is added between the controller and the power converter, then the inverter duty cycles, $d_i[k] \in [0, 1]$, can be considered as the control input of the system. Thus, in this case, the MPC decision variables are continuous, typically resulting in a quadratic program (QP) [29] whose constraints associated to the control inputs have changed from integer variables to linear inequalities. In [31] [32], an explicit model predictive controller (Explicit MPC) for PWM inverters and electrical drives was proposed. This approach is based on a set of locally linear models of the system (piecewise affine model). Applying this strategy, the optimization problem can be solved offline for all regions or elements of this set resulting in a piecewise affine optimal control law as a function of the controller states, i.e. the state space is divided into several convex regions within each one single linear control law is valid. Thus, an optimal explicit piecewise affine solution for each region is obtained. Consequently, the online algorithm is focused on determining which region the system-state belongs.

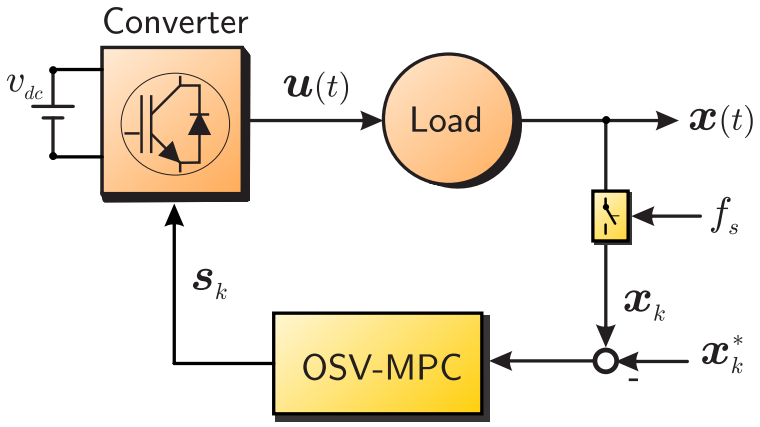

FIGURE 1.6: Optimal Switching Vector MPC (OSV-MPC) block diagram.

In explicit MPC, the weight on the actuator control input is replaced by boundary constraints that represent the real actuator capability. This feature is one of the main differences with the linear quadratic regulator (LQR), where both the tracking error and the control action must be weighted, which considerably increases the tuning effort.

The explicit controller inherits all stability and performance properties of MPC, whereas the online computational effort is reduced drastically.

1.3.2 Finite Control Set Model Predictive Control

A second class of MPC algorithms for power converters is the, so-called, finite control set MPC (FCS-MPC) [30] [33] [34] . This predictive control strategy uses the discrete nature of power converters to simplify the optimization problem of MPC. Thereby, by using the finite set of possible switching states of the power converters, the complexity of the constrained optimization problem can be considerably reduced. Additionally, if the one-step horizon is considered, the optimal problem can be easily solved online, making this strategy one of the most attractive predictive strategies in practice [33].

Depending on the nature of the input constraints, FCS-MPC can be divided into two categories: optimal switching vector MPC (OSV-MPC) and optimal switching sequence MPC (OSS-MPC) [4]. The first one directly uses the switching vectors (SVs) to define the feasible control set. Conversely, the OSS-MPC establishes a set of switching sequences (SSs), each of them composed of a limited number of SVs. Therefore, in general, both MPC strategies perform an enumeration search algorithm in which the predictions of the system over the control set are evaluated into a cost function. Accordingly, the implementation of FCS-MPC based strategies typically produces a high computational burden for the digital control platform.

1.3.2.a Optimal Switching Vector MPC (OSV-MPC)

Fig. 1.6 shows a simplified block diagram of the OSV-MPC strategy. This control method predicts the future behavior of the system for each feasible switching vector $\boldsymbol{s}_k \in \mathcal{U}_s = \{\boldsymbol{s}_1, \ldots, \boldsymbol{s}_w\}$ by means of using the discrete-time model of the system. Generally, this set consists in the power converter output voltage vectors. Then, to obtain the optimal switching vector $\boldsymbol{s}_k^\star \in \mathcal{U}_s$, a suitable cost function is evaluated for all the predicted system trajectories. The SV that minimizes the cost function is the control action to be applied during the whole next sampling period. Consequently, modulation stages are not required.

The main advantage is that the optimal control problem can be easily solved even for multi-objective optimization problems that include system constraints. Nevertheless, since the OSV-MPC directly handles the SVs of the converter, it applies the optimal SV during the whole switching cycle [3, 33]. Therefore, unless additional terms in the objective function or constraints are added to the optimization problem [35, 36], OSV-MPC could lead to the same optimal SV during several consecutive switching cycles. Accordingly, this MPC strategy generates a variable switching frequency, producing a dispersed harmonic spectrum and higher ripple in the waveforms synthesised by the converter, than that produced by techniques that include modulation stages at similar switching frequencies [37].

Therefore, it discourages the adoption of this solution for grid-connected power converter applications, due to the harmonic content constraints imposed by the grid codes [5]. Moreover, OSV-MPC controller produces a nonzero average steady-state tracking error [38, 39]. This disadvantage becomes relevant when the variable to be controlled is the active power to be injected into the grid.

1.3.2.b Multistep FCS-MPC

Multistep FCS-MPC (or FCS-MPC with long horizons) for power electronics has been recently presented in [35], [40]. Here, an efficient optimization algorithm for solving the predictive control problem for very long prediction horizons is presented. The optimization problem is reformulated as a *integer-least-square* problem in order to adapt sphere decoding principles [41] to the underlying optimization problem, and thus, to find efficiently the optimal switching sequence. Nevertheless, the optimization problem still has a discrete domain space, and therefore, it is an NP-hard problem [42], [43]. The method is illustrated for a variable speed drive system with a three-level NPC (3L-NPC) voltage source converter.

Using sphere decoding, the optimization problem for FCS-MPC with long prediction horizons such as 10 can be solved relatively quickly. However, the maximum number of nodes to be investigated in each sampling period has not a deterministic upper bound that guarantees the algorithm execution during the available time. An empirical maximum number of nodes is shown for different prediction horizons. They indicate that in 95% of the cases fewer than 85 nodes need to be explored. For this practical application, the multistep predictive control approach provides signif-

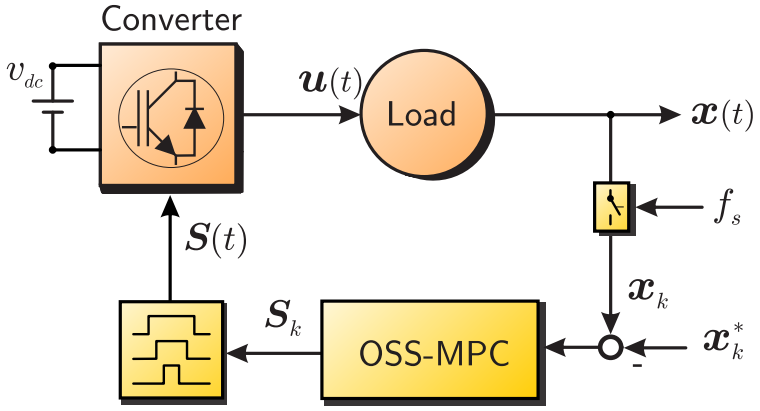

FIGURE 1.7: Optimal Switching Sequence MPC (OSS-MPC) block diagram.

icant performance benefits. Indeed, the current distortion and/or the switching frequency can be reduced considerably with respect to FCS-MPC. Therefore, better performance than direct MPC is obtained in steady-state without losing its good transient properties. Recently in [36], the Multistep MPC strategy was applied to Cascaded H-Bridge Inverters. In this work, to reduce the computational effort introduced by a long prediction horizon implementation, this MPC formulation is transformed into an equivalent optimization problem that can be solved by a fast sphere decoding algorithm. Moreover, the benefits of including the control input references in the proposed formulation are analyzed based on this equivalent optimization problem. Experimental results show that the proposal provides an improved steady-state performance in terms of current distortion, inverter voltages symmetry, and common-mode voltage.

1.3.2.c Optimal Switching Sequence MPC (OSS-MPC)

As reported in the literature [44–50], to overcome some of the difficulties of the standard OSV-MPC, the OSS-MPC strategy determines the commutation instants (within a switching cycle) of a limited number of SVs.

The OSS-MPC strategy consists of defining the control set by employing a limited number of possible switching sequences. Similar to OSV-MPC strategy, the optimal switching sequence (OSS) is selected from a finite set of switching sequences which in turn are composed of a limited number of SVs. Thus, the optimal control problem is formulated by considering the instant where the switching vector changes from one state to another one, which in a way embeds the modulator into the optimization problem. Thus, a suitable modulation scheme is typically integrated into the OSS-MPC strategy to emulate the desired switching sequence easily.

In [44], a heuristic based control strategy is introduced to compute the duty cycles related to the zero and active vectors of a two-level voltage source converter (2L-VSC). The controller is named modulated MPC, and it is able to operate with fixed switching frequency maintaining the inherent fast dynamic of the OSV-MPC. This kind of controller is extended in [48] for a grid-connected

3L-NPC converter. However, due to some oversimplifications in the formulation of the problem, this strategy introduces low-frequency harmonics for either low modulation indexes or a relatively small sampling frequency [48].

A control scheme that also combines MPC and PWM techniques was introduced in [49] for a 2L-VSC based permanent magnet synchronous machine drive. In this strategy, the tracking error produced by each SV is evaluated using a quadratic cost function. The two active vectors leading to the lowest costs are selected, and their duty cycles are then computed by solving a system of linear equations which is derived from a geometrical analysis. Because of its structure, the resulting algorithm behaves as a multi-variable deadbeat controller. Therefore, considering modelling errors, unmodeled delays, and external disturbance, this controller may produce a deteriorate closed-loop performance [29]. This work was recently extended in [50] to consider the overmodulation region of the 2L-VSC.

A constrained optimization problem (COP) has been addressed in [45] for model predictive direct power control of 2L-VSCs. This work is improved in [46], by solving the associated COP for the six sectors in which the control region is typically divided. This provides six local optimal switching sequences (OSSs) and their associated cost values. A similar extended methodology is used in [47] for the grid current control of a single-phase full-bridge NPC converter. Experimental results show the desired fixed switching behavior in steady-state condition and the intrinsic fast dynamic provided by OSV-MPC during transients. However, sub-optimal commutation instants are provided by these controllers during transient operating conditions, in which the non-negative constraint is violated for every local solution. Moreover, the dc-link capacitor balancing problem has not been addressed in [47].

1.4 Motivation

As mentioned earlier, the OSS-MPC presents two main advantages. First, it provides fixed switching frequency and well-defined harmonic spectrum of the inverter output voltages, making the approach suitable for grid-connected power converter applications. Second, it allows working with a multi-objective optimization problem, including system constraints. Nevertheless, there still remain some unwanted features and issues to be improved [44] [49] [50] [47]. They are listed below:

1. Optimal application times are only provided under steady-state operating conditions. During transients, several heuristic methods have been proposed in the literature to provide feasible solutions. Consequently, sub-optimal duty cycles are provided by the OSS-MPC strategies during transient operating conditions.

2. OSS-MPC algorithm provides, in general, a nonzero average steady-state tracking error. Therefore, the system trajectory may converge to a bounded region around the reference, but not precisely to the reference. This comes from the fact that the control target is to reduce

the gap between the instantaneous value of the variables to be controlled and their references at the end of the switching cycle, following the philosophy of the standard OSV-MPC strategy.

3. The multiple-objective model predictive control and its performance depends on the weighting factors design, which in general, it is a nontrivial process. Moreover, the system performance depends on the operating points and its parameters. Although by theory, the overall multi-objective model-predictive control problem has a unique, globally optimal solution, this does not imply optimality of each sub-performance index [51], [52]. Therefore, the combination of two or more objectives in a single cost function should be avoided.

4. In general, FCS-MPC algorithms require a significant amount of computations. Additionally, by comparing OSS-MPC and OSV-MPC, the former has a higher computational burden mainly because it solves a continuous optimal control problem over a finite set of switching sequences. Moreover, full enumeration algorithms are reported in the literature to obtain the optimal switching sequence.

1.5 General Problem Description

This work presents a new OSS-MPC strategy for grid-connected 3L-NPC converters that does not use weighting factors to trade-off the primary control target with the balancing of the capacitor voltages. The proposed control strategy is formulated for the grid current control, and then it is extended for direct power control with the concerning of fulfilling the power quality requirements imposed by more stricter and demanding grid codes.

This strategy is called Cascaded Optimal Switching Sequence Model Predictive Control (C-OSS-MPC), and it introduces two well-formulated COPs to optimally achieve each control goal separately avoiding all the problems and difficulties related to the design of the weighting factors.

1.6 Project Hypotheses

The predictive control approaches proposed in this work for power converters introduce the following improvements and more relevant features:

- C-OSS-MPC fixes the switching frequency achieving a well-defined harmonic spectrum of the inverter output voltage.

- C-OSS-MPC maintains the good dynamic responses of the standard OSV-MPC strategy, even if the control algorithm is implemented with low sampling period.

- C-OSS-MPC reduces the steady-state tracking error by implemented symmetrical switching

sequences with a cost function focusing on the average tracking error during a switching cycle instead of the instantaneous error at the end of the switching cycle

- C-OSS-MPC provides the optimal application times of any SVs belonging to a finite set of predefined switching sequences even during transient operating conditions.
- C-OSS-MPC can be implemented in a practical digital platform based on DSP and FPGA.
- C-OSS-MPC can be extended for the control of the induction machine with several model predictive control approaches such as direct current control, flux control and, direct torque control.

1.7 Project Objectives

This Ph.D research aims to investigate the operation of grid-connected 3L-NPC converters for integration of renewable energy resources into the main utility. The research described in this thesis pursues to accompplish the following objectives:

- To propose MPC methodologies to allow the operation of the grid-connected 3L-NPC converter with fixed switching frequency and well-defined harmonic spectrum of the inverter voltages avoiding the use of weighting factors to balancing the capacitor voltages.
- To propose a computationally efficient OSS-MPC algorithm which can be implemented in an actual digital platform and also that allows the control strategy to be applied to another multilevel converters topologies.
- To implement a downscale 3L-NPC converter prototype to validate the proposed control strategies for grid-connected power converter applications. Experimental validation includes 3L-NPC converters feeding a passive load to obtain performance indexes over the whole range of modulation indexes.

1.8 Contributions

The contributions of this work can be summarised as follows:

- Two Model Predictive Control Strategies based on Optimal Switching Sequences are proposed to handle grid-connected 3L-NPC power converters.
- A comprehensive formulation of the proposed OSS-MPC strategy which embeds the modulation stage in the optimal control problem.

- The proposed control strategy takes advantage of the symmetric nature of the switching sequences to reduce the average tracking error during each switching cycle.

- The proposed Cascaded-OSS-MPC strategy introduces two well-formulated control optimal problems to optimally control both the primary control target (grid-current or active/reactive power) and the capacitor voltages balancing even during large disturbances and step-changes in the references.

- An efficient control algorithm is also addressed to reduce the computational burden typically observed in OSS-MPC strategies. Furthermore, the control algorithm can be extended and applied to other multilevel topologies.

- A very simple reduced order grid-voltage observer is introduced in this research effort to remove the distortion in the utility voltage waveform due to the high-frequency grid-current ripple. This observer allows estimating the grid-voltage vector using just one voltage transducer.

- Experimental validation of the proposed control strategies is provided, including current control, direct active/reactive power control, and capacitor voltages. In all cases, the proposed Cascaded-OSS-MPC strategies perform excellent steady-state and transient response.

CHAPTER 2

Background Theory

This chapter provides the theoretical background and principle of operation of three-level NPC converters. Furthermore, this chapter focuses on introducing the main features of this VSC topology and the modulation schemes widely used to handle them, highlighting several switching sequences which are applied during a sampling period and the capacitor voltage balancing problem.

Furthermore, this chapter provides a brief review of the instantaneous power theory and standard control schemes for grid-connected power converter applications.

Finally, the maximum harmonic current injection into the grid is also introduced regarding the Standards IEEE-519 and IEEE 1547.

2.1 Grid-Connected Power Converters

Grid-connected power converters play a crucial role in distributed generation and integration of renewable energy sources into the electrical grid. It is also widely employed in many industrial applications such as energy storage systems, active-front-end rectifiers and power conditioning units [53, 54].

Several converter topologies, grid synchronization schemes, power quality standards, and modulation and control algorithms have been studied in literature to improve the overall performance of grid-tied power converters [55].

Control strategies for power converters have been constantly evolving according to the development of new semiconductor devices and the introduction of new control platforms [29]. Control methodologies commonly applied in grid-connected power converters are classified as direct or indirect control techniques [55–64]. The most widely used indirect strategy is voltage-oriented control [55] where the powers set points are mapped into equivalent set points for the currents in a synchronous reference frame oriented along the grid voltage vector. Indirect control strategies usually lead to good transient behaviour and acceptable steady-state operation. They operate at a constant switching frequency due to the integration of a modulation stage within the control process. Thus, the design of the line-side filter and cooling systems are simple to optimize [65].

Direct Power Control (DPC) is a popular scheme for the control of grid-connected power converters. DPC methodology directly controls the instantaneous active and reactive power by selecting the switching states of the converter without using any inner-loop current regulators [57–64]. As described in [57], in the standard approach, the optimal switching actions are obtained by utilizing a lookup table and hysteresis bounds.

Fig. 2.1 depicts a typical grid-connected VSC for interfacing a renewable energy resources

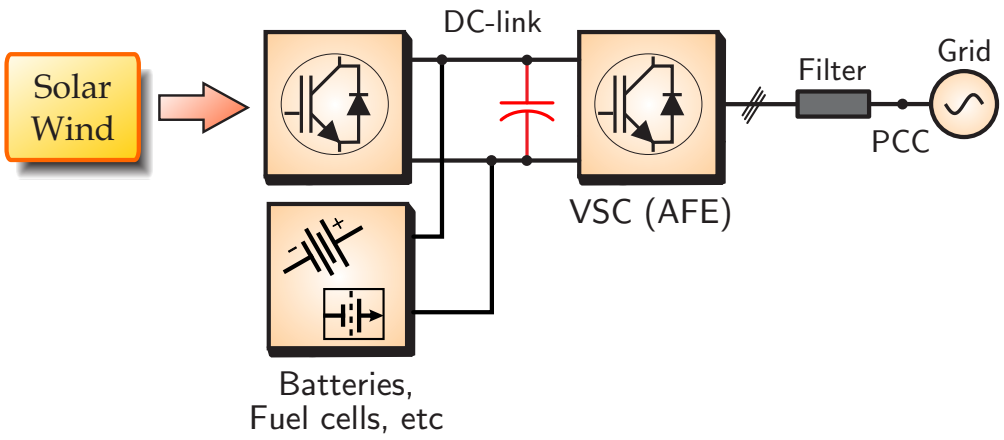

FIGURE 2.1: Renewable energy resource injecting electrical power into the grid.

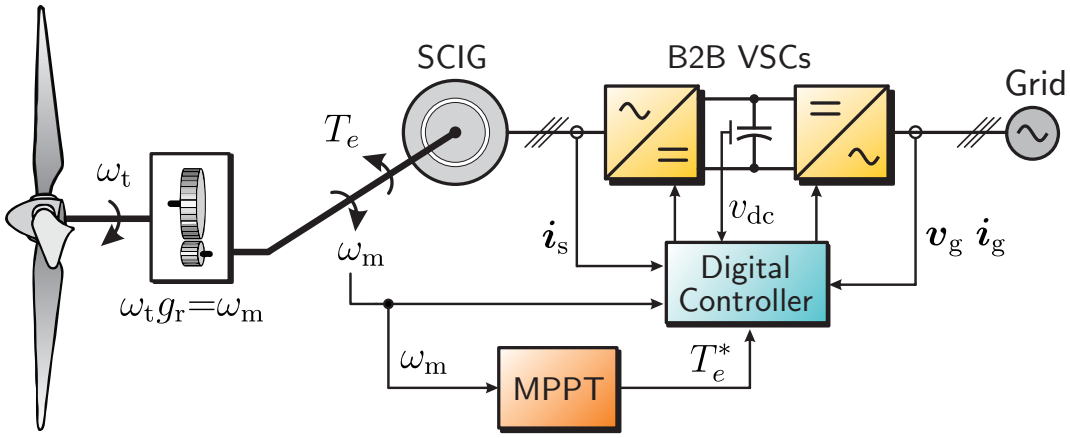

FIGURE 2.2: Full-scale squirrel cage induction generator (SCIG) based WECS.

(RER) into the main utility. Different power converter topologies are used for feeding the inverter stage depending on the RER installed. For instance, in photovoltaic energy conversion system, DC-DC power converters are utilized for feeding the inverter stage. On the other hand, in wind energy conversion systems (WECSs), the machine-side is typically fed by a VSC in rectifier mode which enables the back-to-back topology, as shown in Fig. 2.2 for a full-scale squirrel cage induction generator based WECS..

The grid-connected power converter (also known as active front-end (AFE) rectifier) allows the control of the active and reactive power that is delivered to the grid by the electrical drive [66]. A typical nested control system for the grid-side converter is shown in Fig. 2.3. Here, the inner control loop is designed for controlling the grid current whose references are obtained from the dc-link voltage and reactive power external control loops.

2.1.1 The Instantaneous Active and Reactive Power

To formulate grid-connected converter control strategies, the instantaneous dynamic relations of the grid and the converter are defined in terms of their respective currents and voltages with a convenient usage of the $\alpha\beta 0$ transform given in (2.19) [67] .

Thereby, by employing the vector representation of the grid currents and voltages respectively as $\boldsymbol{i}_g = \begin{bmatrix} i_{g\alpha} & i_{g\beta} \end{bmatrix}^\intercal$ and $\boldsymbol{v}_g = \begin{bmatrix} v_{g\alpha} & v_{g\beta} \end{bmatrix}^\intercal$, and considering the grid as the instantaneous active and reactive power at the point of common coupling (PCC) for a three-phase three-wire system can be determined respectively as [67]:

$$p_g = \frac{3}{2}(v_{g\alpha} i_{g\alpha} + v_{g\beta} i_{g\beta}) \tag{2.1a}$$

$$q_g = \frac{3}{2}(v_{g\beta} i_{g\alpha} - v_{g\alpha} i_{g\beta}) \tag{2.1b}$$

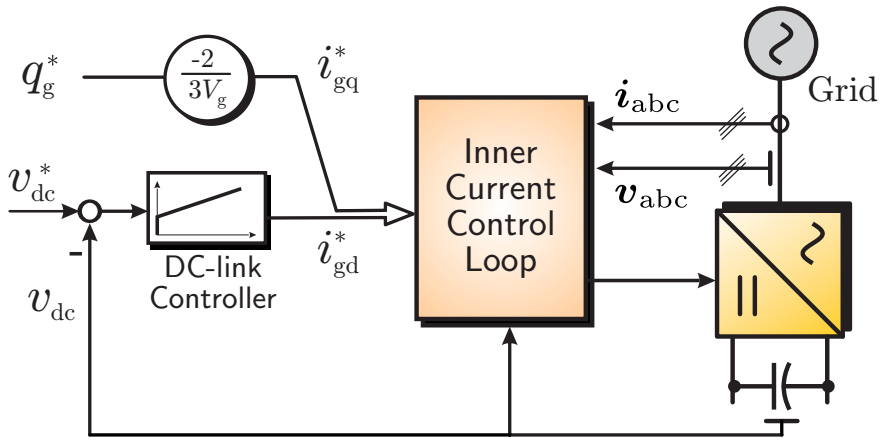

FIGURE 2.3: Indirectly power control of grid-connected converters

It is straightforward to demonstrate that both active and reactive power can be manipulated by handling the grid current vector since the grid voltage is imposed by the AC power system. Under this perspective, the grid currents are usually controlled in order to regulate the active and reactive power flow. Therefore, for a given voltage vector $\boldsymbol{v}_{\mathrm{g}}$, the grid current vector required for injecting the desired active and reactive power p_{g}^* and q_{g}^* can be computed as

$$\begin{bmatrix} i_{\mathrm{g}\alpha}^* \\ i_{\mathrm{g}\beta}^* \end{bmatrix} = \frac{2}{3}\frac{1}{V_{\mathrm{g}}^2}\begin{bmatrix} v_{\mathrm{g}\alpha} & v_{\mathrm{g}\beta} \\ v_{\mathrm{g}\beta} & -v_{\mathrm{g}\alpha} \end{bmatrix}\begin{bmatrix} p_{\mathrm{g}}^* \\ q_g^* \end{bmatrix} \tag{2.2}$$

where $V_{\mathrm{g}}^2 = v_{\mathrm{g}\alpha}^2 + v_{\mathrm{g}\beta}^2$.

On the other hand, if the control strategy is established in a synchronous reference frame (SRF) oriented along the grid voltage vector (usually known as voltage oriented control [68]), the active and reactive powers in (2.1) can be rewritten in term of the d- and q-axis currents according to

$$p_{\mathrm{g}} = \frac{3}{2}V_{\mathrm{g}}i_{\mathrm{gd}} \tag{2.3}$$

$$q_{\mathrm{g}} = -\frac{3}{2}V_{\mathrm{g}}i_{\mathrm{gq}} \tag{2.4}$$

Hence, for the grid-connected converter shown in Fig. 2.3, the d-axis grid current (i_{gd}) is employed to regulate the dc-link voltage, and thus indirectly controls the active power injected by the energy resource. Besides, the q-axis grid current (i_{gq}) establishes the reactive power injected or absorbed into the grid and thus, unity power factor operation can also be established by using the reactive power command equal to zero, i.e., $q_g^* = 0$.

To ensure a proper operation of the VOC strategy, the angular position of the grid voltage vector has to be precisely computed even more during unbalanced conditions. Under this perspective, a robust and efficient phase-locked loop (PLL) has to be implemented within the VOC control

algorithm [69] [70] [8].

The use of a stationary ($\alpha\beta$-axis) or synchronous reference frame (dq-axis) based control strategy depends on the type of controllers used in the inner control loop (usually a current control loop). Thereby, when low bandwidth controllers are implemented, i.g., PI controllers, the SRF is mandatory to ensure a zero steady-state tracking error. On the other hand, proportional resonant controllers (PRs) have emerged as an attractive alternative mainly because of both the positive and negative symmetrical components can be directly controlled with just one PR controller when the grid voltage is unbalanced [71]. Unlike these linear controllers, the FCS-MPC can be directly implemented in both coordinate systems [72].

2.1.2 Dynamic model

To design a suitable controller for the regulation of the line currents of a grid-connected power converter, the dynamic model of the grid current vector has to be derived first. The required model will depend on the type of filter used at the output of the inverter (L-type or LCL-type filter). However, the influence of the capacitor of the filter can be neglected since it only deals with the switching ripple frequencies [8]. Indeed, at frequencies lower than half of the resonance frequency, the LCL-filter based inverter behaves as if the capacitor is not present and the frequency response is equivalent to the frequency characteristic of L-filter made by the sum of the inductances of the LCL filter [8]. Thus, the dynamic of the line currents is governed by the following equation in the $\alpha\beta$ frame

$$\frac{\mathrm{d}\boldsymbol{i}_{\mathrm{g}}}{\mathrm{d}t} = -\frac{R}{L}\boldsymbol{i}_{\mathrm{g}} + \frac{1}{L}(\boldsymbol{v}_s - \boldsymbol{v}_{\mathrm{g}}), \tag{2.5}$$

where $\boldsymbol{v}_s$ and $\boldsymbol{v}_{\mathrm{g}}$ are, respectively, the converter and grid voltage vectors, while L and R are the overall parameters of the output filter.

On the other hand, it is well-known that any vector rotating on the $\alpha\beta$ frame $\boldsymbol{x}_{\alpha\beta}$ can be expressed on a synchronous reference frame $\boldsymbol{x}_{dq}$ by employing the following transformation

$$\boldsymbol{x}_{dq} = \mathbf{T}_{\mathrm{dq}}(\theta)\boldsymbol{x}_{\alpha\beta} \tag{2.6}$$

where the rotation matrix and its inverse are defined as

$$\mathbf{T}_{\mathrm{dq}}(\theta) = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \quad ; \quad \mathbf{T}_{\mathrm{dq}}^{-1}(\theta) = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \tag{2.7}$$

In (2.7), the angle θ is the angular position of the orthogonal dq-axes in the $\alpha\beta$ plane which are rotating at frequency $\omega = \dot{\theta}$. Hence, as the orthogonal reference frame is rotated by θ from $\alpha\beta$ to dq in a counterclockwise direction, the vector $\boldsymbol{x}_{\alpha\beta}$ must be rotating in opposite direction (clockwise direction) to transform it into $\boldsymbol{x}_{dq}$.

Thus, the AC voltage equilibrium equations (2.5) expressed in the dq frame, which is synchro-

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order (odd harmonics)[a, b]						
I_{SC}/I_L	$3 \le h < 11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h \le 50$	TDD
< 20[c]	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

FIGURE 2.4: Current distortion limits for systems rated 120 V through 69 kV [5], where I_{SC} is the maximum short-circuit current at PCC, and I_L is the maximum demand load current.

nised with the grid voltage vector, are

$$\frac{\mathrm{d}\boldsymbol{i}_\mathrm{g}}{\mathrm{d}t} + \mathbf{J}\omega_\mathrm{g}\boldsymbol{i}_\mathrm{g} = -\frac{R}{L}\boldsymbol{i}_\mathrm{g} + \frac{1}{L}(\boldsymbol{v}_s - \boldsymbol{v}_\mathrm{g}), \tag{2.8}$$

with

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{2.9}$$

Therefore, either (2.5) or (2.8) can be used depending on the nature of the controller adopted for the inner current closed loop.

2.2 Current Harmonic Requirements

In the last years, as mentioned earlier, the integration of distributed energy resources into electric power systems has been emerging as a critical issue driven by environmental motivations and economical stimulus. This fact has imposed technical and technological significant challenges concerning reliability, stability and electric power quality. Under this perspective, the impact of grid-connected power converters becomes more significant [7] [8].

Power quality requirements have been mainly developed in order to preserve the quality of the grid voltage waveform in amplitude, frequency and phase [8]. The main perturbation to the voltage waveform are due to system transient operation (e.g. at start-up of high power induction motors) or to power fluctuations (due to the uncertainty of some primary energy sources). However, the quality of the injected current is also of concern, and in this sense, the grid-connected converter is the main responsible for compliance with power quality international recommendations and standards as well as the requirements imposed by the transmission system operators [5] [73].

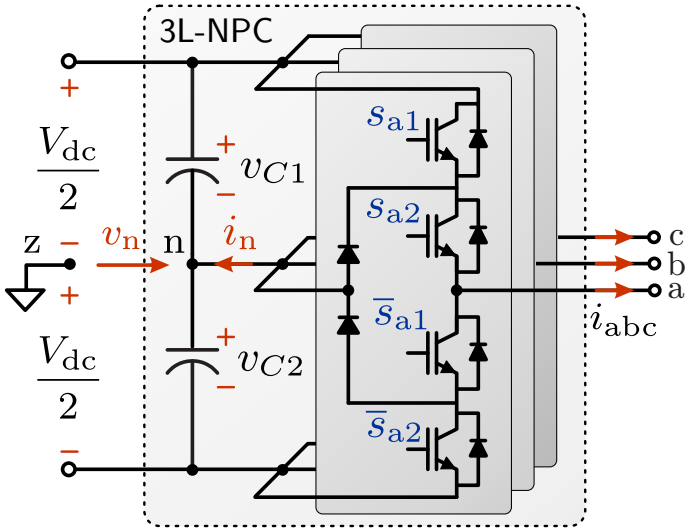

FIGURE 2.5: The three-level NPC converter topology.

The current injected into the grid should not have a total demanded distortion (TDD) larger than 5%. For the grid-current, the TDD is defined as

$$I_{\mathrm{TDD}} = \frac{1}{\sqrt{2} I_{\mathrm{nom}}} \sqrt{\sum_{h \neq 1} I_{\mathrm{g},h}^2} \tag{2.10}$$

where $I_{\mathrm{g},h}$ refers to the nominal grid current and, $I_{\mathrm{g},h} \geq 0$ are the amplitudes of the current harmonics at frequencies hf_1. To compute the TDD of a three-phase current, the TDD is computed for each of the a, b, and c phase currents separately. The overall TDD is then determined by taking the mean value of the three phases.

A detailed image of the harmonic distortion regarding each harmonic component is given in Fig. 2.4, as recommended by [5]. For distributed resources, the first row in Fig. 2.4 is commonly utilised, in which the ratio between the maximum short-circuit current and the maximum demand current at the PCC is below to 20, i.e., $I_{SC}/I_L < 20$.

2.3 The Three-level Neutral Point Clamped VSC

The three-level neutral point clamped (3L-NPC) VSC, also known as the three-level diode-clamped converter, was introduced in 1981 [14] and nowadays has become into a standard topology for high-power and medium-voltage (MV) applications (up to a range of 4.16kV) [74] [75]. Compared to the 2L-VSC, the 3L-NPC converter offers several advantages, such as: reduction of the dv/dt and the corresponding Electromagnetic Interference (EMI), improvement of the output harmonic spectrum because of its three-level nature, reduction of the switching frequency per device and, maybe its main feature, distribution of the device blocking voltage, where, ideally, each device of

the converter withstand only half of the dc-link voltage.

The circuit diagram of a 3L-NPC converter is shown in Fig. 2.5. It is composed of two additional diodes and semiconductor devices (IGBT or IGCT) per leg when compared to the 2L-VSC. The clamped diodes link the midpoint of the main switches to the neutral-point of the converter "n". Thus, the connection of the phase output $\mathrm{x} \in \mathcal{P} = \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$ to the converter neutral-point enables the three-level characteristic of the topology. As illustrated in Fig. 2.5, the dc-link is split by two capacitors, denoted as C_1 and C_2. For the proper operation of the 3L-NPC converter, the capacitor voltages should be operating balanced with a reduced voltage ripple.

2.3.1 Principle of Operation

The three output voltage levels considering the capacitors are balanced to the half of the dc-link voltage are depicted in Fig. 2.6. As shown in Fig. 2.6(a), when the upper switches are closed, i.e., when the gate signals are $(s_{\mathrm{x1}}, s_{\mathrm{x2}}) = (1, 1)$, the output voltage measured from the dc-link middle point is $v_{\mathrm{xn}} = V_{\mathrm{dc}}/2$. This switching state is often named as P-type switching state. Similarly, as shown in Fig. 2.6(b), when the middle switches are closed, i.e., $(s_{\mathrm{x1}}, s_{\mathrm{x2}}) = (0, 1)$, the output voltage is $v_{\mathrm{xn}} = 0$ and thus, it is called as a 0-type switching state. Finally, when the lower switches are closed, i.e., $(s_{\mathrm{x1}}, s_{\mathrm{x2}}) = (0, 1)$, the N-type switching state is produced and the output voltage is $v_{\mathrm{xn}} = -V_{\mathrm{dc}}/2$, as is shown in Fig. 2.6(c). Therefore, each switching state can be represented by the variable $u_{\mathrm{x}} \in \{-1, 0, 1\}$.

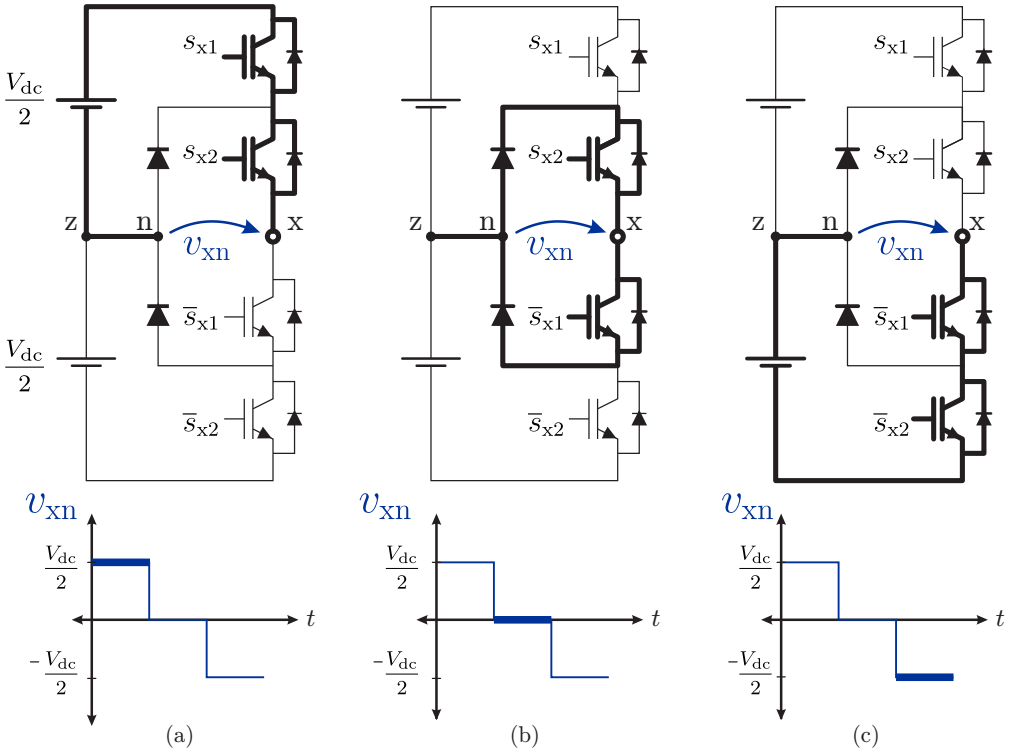

FIGURE 2.6: One-leg 3L-NPC converter switching states.

Table 2.1 summarizes the operating modes, switching states and the neutral-point current i_{n} (whose polarity is defined in Fig. 2.5) when the 3L-NPC converter operates with their capacitor voltages balanced.

TABLE 2.1: Phase Leg switching states of a 3L-NPC converter

Gate signals (s_{x1}, s_{x2})	**Switching state** u_{x}	**Output voltage** v_{xn}	**NP-current** i_{n}
$(1,1)$	$+1$	$V_{dc}/2$	0
$(0,1)$	0	0	$-i_{\mathrm{x}}$
$(0,0)$	-1	$-V_{dc}/2$	0

2.3.2 Mathematical Model

According to the circuit diagram shown in Fig. 2.5, the three-phase inverter voltages $\boldsymbol{v}_{\mathrm{abc}} = \begin{bmatrix} v_{\mathrm{az}} & v_{\mathrm{bz}} & v_{\mathrm{cz}} \end{bmatrix}^{\intercal}$ (measurement respect to the dc-link middle point) can be expressed in term of the switching states $\boldsymbol{u}_{\mathrm{abc}} = \begin{bmatrix} u_{\mathrm{a}} & u_{\mathrm{b}} & u_{\mathrm{c}} \end{bmatrix}^{\intercal}$ according to

$$\boldsymbol{v}_{\mathrm{abc}} = \frac{1}{2} V_{\mathrm{dc}} \boldsymbol{u}_{\mathrm{abc}} + (1 - |\boldsymbol{u}_{\mathrm{abc}}|) v_{\mathrm{n}} \tag{2.11}$$

where $|\boldsymbol{u}_{\mathrm{abc}}| = \begin{bmatrix} |u_{\mathrm{a}}| & |u_{\mathrm{b}}| & |u_{\mathrm{c}}| \end{bmatrix}^{\intercal}$ is the component-wise absolute value of the switching states and, v_{n} is the neutral-point voltage (NP-voltage). As illustrated in Fig. 2.5, this voltage represents the imbalance level of the converter due to it is defined as

$$v_{\mathrm{n}} = \frac{1}{2}(v_{C2} - v_{C1}) \tag{2.12}$$

Applying Kirchhoff's laws to the circuit diagram shown in Fig. 2.5, the following dynamic equations can be stated for the capacitor voltages:

$$C_2 \frac{\mathrm{d}v_{C2}}{\mathrm{d}t} - C_1 \frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = i_n \tag{2.13}$$

$$\frac{\mathrm{d}v_{C2}}{\mathrm{d}t} + \frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = \frac{\mathrm{d}V_{\mathrm{dc}}}{\mathrm{d}t}. \tag{2.14}$$

Consequently, the dynamic model for the NP-voltage is given as follows:

$$\frac{\mathrm{d}v_{\mathrm{n}}}{\mathrm{d}t} = \frac{1}{C_1 + C_2} i_{\mathrm{n}} + \frac{1}{2} \frac{C_1 - C_2}{C_1 + C_2} \frac{\mathrm{d}V_{\mathrm{dc}}}{\mathrm{d}t} \tag{2.15}$$

Therefore, if the capacitances are equal or the dc-link voltage is invariant in time, the NP-voltage evolves as a function of the NP-current i_{n} according to

$$\frac{\mathrm{d}v_{\mathrm{n}}}{\mathrm{d}t} = \frac{1}{C_1 + C_2} i_{\mathrm{n}}. \tag{2.16}$$

Furthermore, because of only the 0-type switching state transfers the phase-current to the neutral-point of the converter, the NP-current can be mathematically expressed in term of the phase leg switching state $u_{\mathrm{x}} \in \{-1, 0, 1\}$ as

$$i_{\mathrm{n}} = \sum_{\mathrm{x} \in \mathcal{P}} (|u_{\mathrm{x}}| - 1) i_{\mathrm{x}} \quad \text{with} \;\; \mathcal{P} = \{\mathrm{a}, \mathrm{b}, \mathrm{c}\} \tag{2.17}$$

Moreover, if a three-phase load with floating neutral is considered, $i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}} = 0$ holds; and thus, the NP-current can be rewritten in a vector form as

$$i_{\mathrm{n}} = |\boldsymbol{u}_{\mathrm{abc}}|^{\intercal} \boldsymbol{i}_{\mathrm{abc}}. \tag{2.18}$$

where $|\boldsymbol{u}_{\mathrm{abc}}| = \begin{bmatrix} |u_{\mathrm{a}}| & |u_{\mathrm{b}}| & |u_{\mathrm{c}}| \end{bmatrix}^{\intercal}$ is the component-wise absolute value of the switching states, and $\boldsymbol{i}_{\mathrm{abc}} = \begin{bmatrix} i_{\mathrm{a}} & i_{\mathrm{b}} & i_{\mathrm{c}} \end{bmatrix}^{\intercal}$, the three-phase current as depicted in Fig. 2.5.

As it is concluded from (2.16) and (2.18), the NP-voltage depends on the instantaneous load current as well as the switching states of the converter.

2.3.3 Space of Vectors

Considering that each leg of the converter produces three possible switching combinations, the three-phase 3L-NPC converter has $3^3 = 27$ different switching states in the abc frame denoted as $\boldsymbol{u}_{\mathrm{abc}} \in \{-1, 0, 1\}^3$.

The $\alpha\beta 0$ transformation or the Clarke transformation [67] allows the mapping of the three-phase instantaneous variables in the abc frame into the instantaneous variables on the $\alpha\beta 0$ axes. The amplitude invariant version of this transformation is defined by the following matrix:

$$\mathbf{T}_{\alpha\beta 0} \triangleq \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.19}$$

Therefore, a given switching state in the original frame $\boldsymbol{u}_{\mathrm{abc}} = \begin{bmatrix} u_{\mathrm{a}} & u_{\mathrm{b}} & u_{\mathrm{c}} \end{bmatrix}^{\intercal}$ can be mapped into the $\alpha\beta 0$ frame as $\boldsymbol{u}_{\alpha\beta 0} = \mathbf{T}_{\alpha\beta 0} \boldsymbol{u}_{\mathrm{abc}}$.

To derive the relation between the switching vectors and switching states, a three-phase system

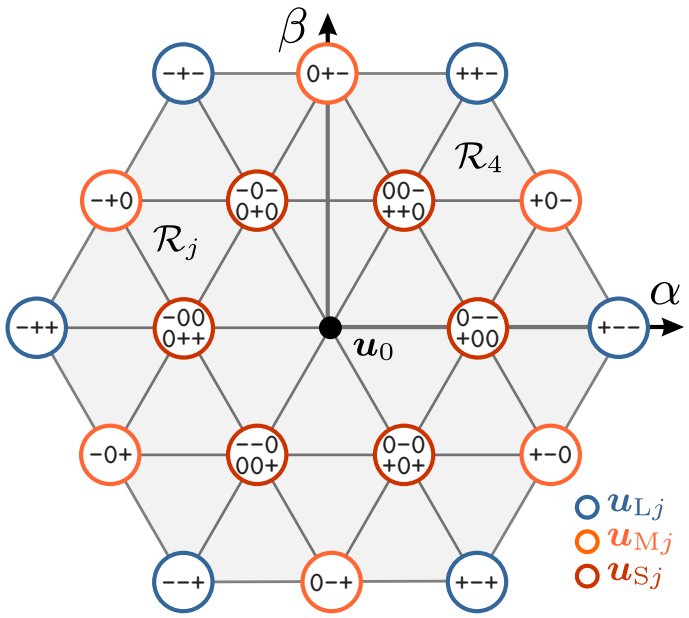

FIGURE 2.7: 3L-NPC converter switching states vectors in the $\alpha\beta$ plane.

with floating neutral is assumed. Hence, the 0-component (commonly known as the common-mode signal) does not affect the three-phase currents. Under this perspective, it is possible to transform the three-phase system into an equivalent two-phase system by employing the following transformation:

$$\boldsymbol{u}_s = \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \underbrace{\frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{\triangleq \mathbf{T}_{\alpha\beta}} \begin{bmatrix} u_{\mathrm{a}} \\ u_{\mathrm{b}} \\ u_{\mathrm{c}} \end{bmatrix} \tag{2.20}$$

Applying the transformation $\mathbf{T}_{\alpha\beta}$ to $\boldsymbol{u}_{\mathrm{abc}}$, only 19 non-redundant switching vectors are produced by the 27 three-phase switching states of the converter. As depicted in Fig. 2.7, the resulting switching vectors are grouped according to its longitude as *zero*, *small* (red), *medium* (orange) and *large* (blue) vectors. They are denoted as $\boldsymbol{u}_0$, $\boldsymbol{u}_{\mathrm{S}}$, $\boldsymbol{u}_{\mathrm{M}}$ and $\boldsymbol{u}_{\mathrm{L}}$, respectively.

Regarding the redundancies, the zero switching vector are produced by three switching positions and hence, they can be represented by $\boldsymbol{u}_0^{\eta_0}$ with $\eta_0 \in \{-, 0, +\}$ (for $\boldsymbol{u}_{\mathrm{abc}} = \{-,-,-\}$, $\{0,0,0\}$ and $\{+,+,+\}$, respectively); on the other hand, each of the six small vectors can be produced by two switching positions. A small vector that connects at least one inverter terminals to the positive dc bus is referred to as *P-type* small vector, whereas the vector connecting at least one output phase to the negative dc bus, is called *N-type* small vector. Therefore, for $j = \{1, \ldots, 6\}$, the small switching vectors are denoted by $\boldsymbol{u}_{\mathrm{S}j}^{\eta_S}$ with $\eta_S \in \{-, +\}$. The medium and large switching vectors do not contain redundancies, and thus each of them is produced by only one three-phase switching state as illustrated in Fig. 2.7.

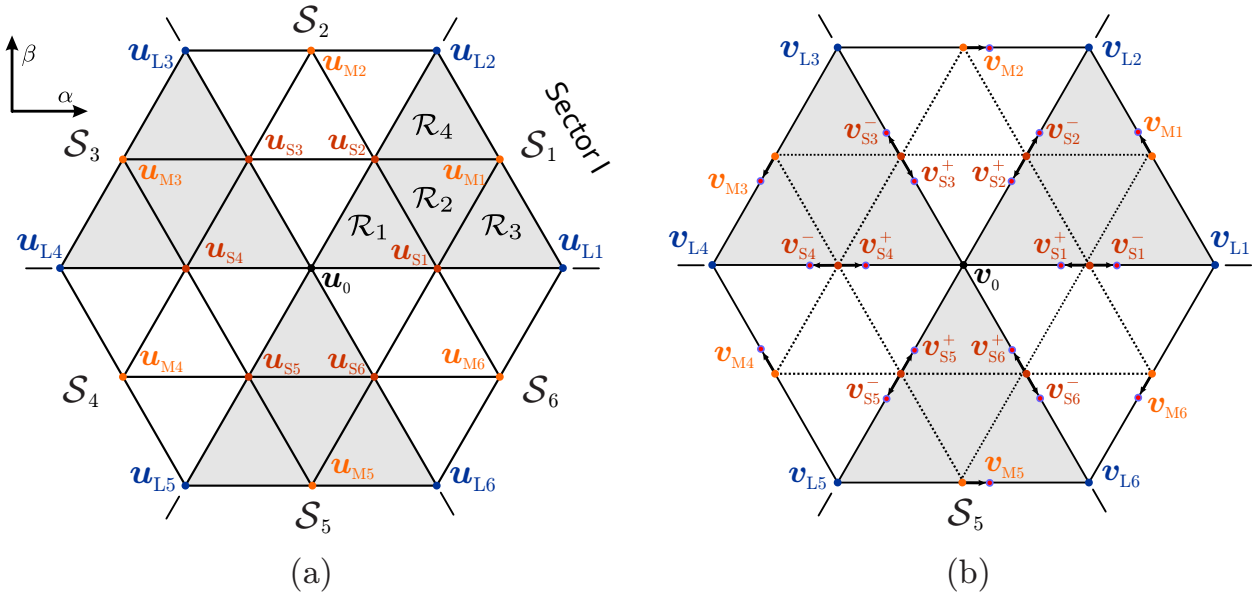

FIGURE 2.8: 3L-NPC space of vectors: (a) switching vectors and; (b) voltage vectors.

To address the influence of the switching vectors in the inverter voltages, the Clark transformation is applied to (2.11). The resulting inverter voltage in the $\alpha\beta$ frame can be therefore expressed in terms of the switching vector as

$$\boldsymbol{v}_{\mathrm{s}} = \frac{1}{2} V_{\mathrm{dc}} \boldsymbol{u}_{\mathrm{s}} - \mathbf{T}_{\alpha\beta} |\boldsymbol{u}_{\mathrm{abc}}| v_{\mathrm{n}}, \tag{2.21}$$

As shown in (2.21), the inverter voltage vector $\boldsymbol{v}_{\mathrm{s}}$ is composed of two components; the first one is the amplified version the switching vector, where the half of dc-link voltage gives the gain and; the second component is proportional to the NP-voltage v_{n}. Thereby, only the small- and medium-size switching vectors are affected by the NP-voltage. As shown in Fig. 2.8, unlike the small switching vectors $\boldsymbol{u}^{\pm}_{\mathrm{S}}$, each small voltage vector and its redundancy $\boldsymbol{v}^{\pm}_{\mathrm{S}}$ do not define a unique point in the $\alpha\beta$ frame. Thus, if the NP-voltage is not zero, the resulting line-to-line inverter voltage is not the same for each pair of small switching vectors.

TABLE 2.2: NP-Current for the 3L- NPC Converter.

Small Vector				Medium Vector	
$\boldsymbol{u}^{+}_{\mathrm{S}}$	i_{n}	$\boldsymbol{u}^{-}_{\mathrm{S}}$	i_{n}	$\boldsymbol{u}_{\mathrm{M}}$	i_{n}
$\{+1,\ 0,\ 0\}$	i_a	$\{\ 0,-1,-1\}$	$-i_a$	$\{+1,\ 0,-1\}$	$-i_b$
$\{+1,+1,\ 0\}$	$-i_c$	$\{\ 0,\ 0,-1\}$	i_c	$\{\ 0,+1,-1\}$	$-i_a$
$\{\ 0,+1,\ 0\}$	i_b	$\{-1,\ 0,-1\}$	$-i_b$	$\{-1,+1,\ 0\}$	$-i_c$
$\{\ 0,+1,+1\}$	$-i_a$	$\{-1,\ 0,\ 0\}$	i_a	$\{-1,\ 0,+1\}$	$-i_b$
$\{\ 0,\ 0,+1\}$	i_c	$\{-1,-1,\ 0\}$	$-i_c$	$\{\ 0,-1,+1\}$	$-i_a$
$\{+1,\ 0,+1\}$	$-i_b$	$\{\ 0,-1,\ 0\}$	i_b	$\{+1,-1,\ 0\}$	$-i_c$

Furthermore, according to (2.18), only small- and medium-size vectors produce a non-zero NP-current i_{n}. Table 2.2 summarizes the NP-current [see i_{n} in Fig. 2.5] considering that $i_{\mathrm{a}}+i_{\mathrm{b}}+i_{\mathrm{c}}=0$.

2.3.4 Switching Sequences

Due to the presence of the redundancies in the space of vectors, several switching sequences (or switching patterns) can be implemented to assembly a desired output voltage vector. Under this perspective, the generation of switching sequences is considered as a degree of freedom that can be used for several purposes such as reduction of switching losses and minimal NP-voltage deviation.

As is reported in the literature, to synthesise a desired inverter output voltage during a switching cycle $T_{\mathrm{s}} = 2T_0$, the three nearest switching vectors are typically employed in carrier-based and space vector PWM techniques [65, 76, 77]. In the context of a three-level NPC converter, the space of vectors is typically divided into six sectors $\mathcal{S}_i$ with $i \in \{1, \ldots, 6\}$, as in the case of the 2L-VSC, and each sector is subdivided into 4 regions as illustrated in Fig. 2.8(a).

Depending on the region where the reference vector is placed, the use of all available redun-

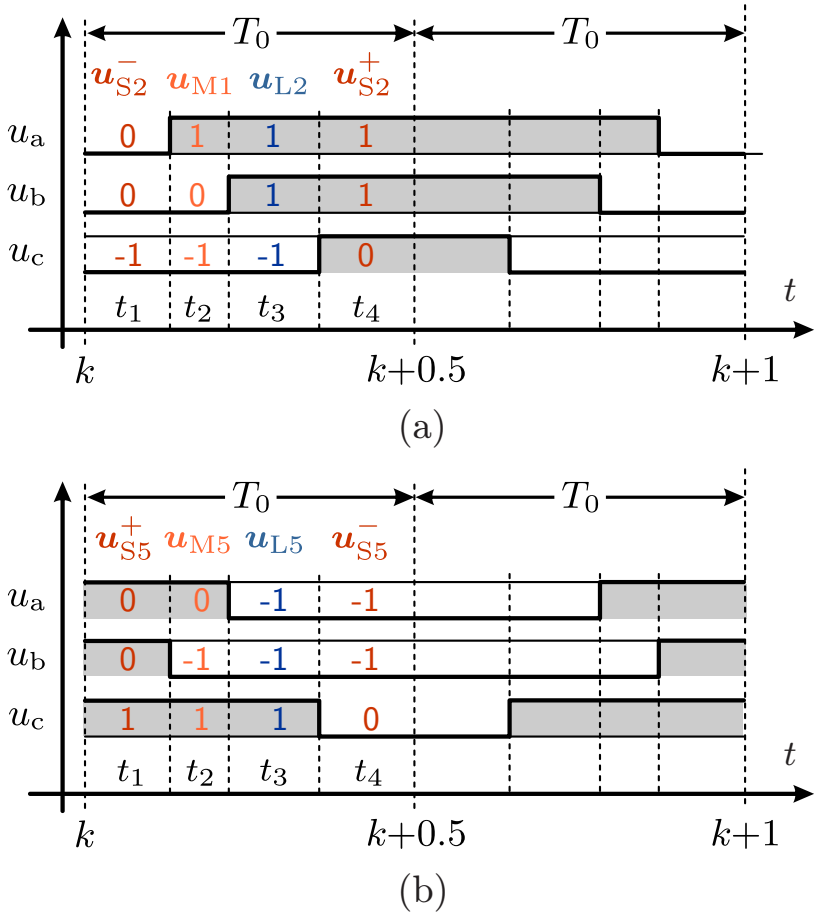

FIGURE 2.9: Seven-segment switching sequences: (a) N-type and; (b) P-type

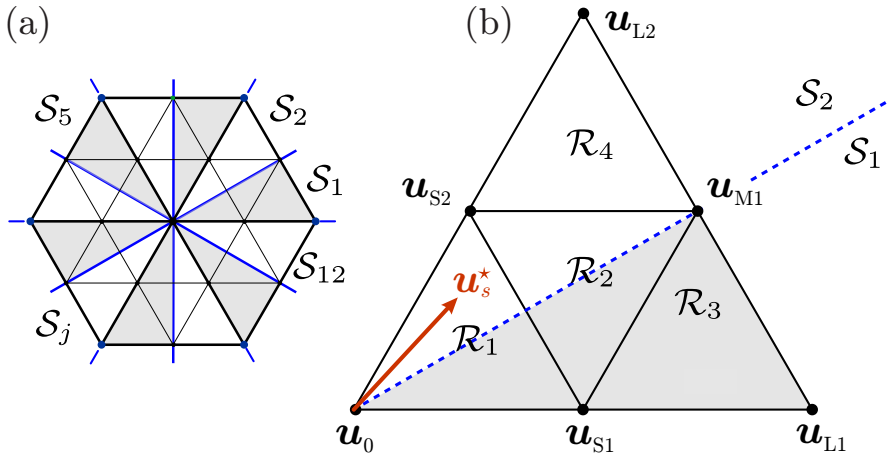

FIGURE 2.10: New partition of the space of vectors based on 12 sectors.

dancies of small and zero switching vectors could produce sequences with an uneven number of commutations, generating different device switching frequencies. This is usually not desired and switching sequences that generate the same switching frequency in every region are commonly implemented. Moreover, switching sequences with direct transitions between the switching states $+1$ and -1 and vice-versa are avoided. In this manner, the number of semiconductor devices being turned on and turned off during a transition from one switching state to the next one is minimized, which certainly reduced the switching losses. Besides, to minimize the NP-voltage deviation, it is desirable to assemble a switching sequence using the small vector redundancy for each region with an even dwell application time distribution between the P- and N-type small switching vectors over a sampling period. The seven-segment symmetric sequence (7S-SS) meets all the above-mentioned features.

The two types of 7S-SSs allowed for the regions 3 and 4 are classified according to the small vector which is used to start the switching sequence. It follows that the *P-type symmetric sequence* starts with a positive small vector $\boldsymbol{u}_{\mathrm{S}}^{+}$, whereas the *N-type symmetric sequence* begins the switching period with a negative small vector $\boldsymbol{u}_{\mathrm{S}}^{-}$. Both sequences use the only redundant switching vector presents in these regions. Fig. 2.9(a) shows the N-type seven-segment symmetric pattern for the region 4 of sector I, and Fig. 2.9(b) shows the P-type sequence for the region 3 of sector 5 as well.

On the other hand, for regions 1 and 2 [see Fig. 2.10(b)] two of the three switching vectors are small vectors; and hence, four possible 7S-SS can be generated by the converter. To reduce the NP-voltage deviation during a switching cycle, each of these two regions is further divided into two sub-regions as illustrated in [see Fig. 2.10(b)]. Thereby, each 7S-SS is implemented with the small vector nearest to the desired switching vector $\boldsymbol{u}_s^\star$ reducing to two the available seven-segment sequences for these regions (one P-type and other N-type). For instance, to synthesize $\boldsymbol{u}_s^\star$ in Fig. 2.10(b), the 7S-SS is executed by using $\boldsymbol{u}_{\mathrm{S2}}$ as dominant small vector instead of $\boldsymbol{u}_{\mathrm{S1}}$. Fig. 2.11 shows the N-type 7S-SS for this example.

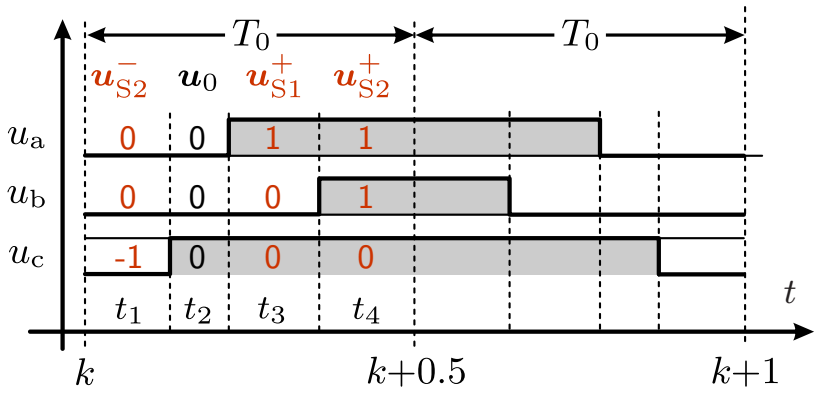

FIGURE 2.11: N-type seven-segment symmetric sequence for region 1 of sector 2.

Therefore, based on the above analysis, the space of vectors can be conveniently partitioned into twelve sections instead of six as illustrated in [see Fig. 2.10(a)]. In consequence, this new partition allows to directly determine the dominant small vector for the region 1 and 2.

2.3.5 Capacitor Voltages Balancing

When a 7S-SS is applied by the converter, the following average model over one switching cycle for the NP-voltage can be derived from (2.16) as

$$(C_1 + C_2)\frac{\mathrm{d}V_\mathrm{n}}{\mathrm{dt}} = \frac{1}{T_\mathrm{s}}\int_{t_k}^{t_k+T_\mathrm{s}} i_\mathrm{n}(t)d\tau \; ; \quad t_k \leq t \leq t_k + T_\mathrm{s} \tag{2.22}$$

Considering that the line currents $\boldsymbol{i}_\mathrm{abc}$ are approximately constant during the time interval $t_k \leq t \leq t_k + T_\mathrm{s}$, the average NP-current given on the right-hand side of (2.22) can be rewritten as

$$I_n = d_\mathrm{S}^+ i_\mathrm{nS}^+ + d_\mathrm{x} i_\mathrm{nx} + d_\mathrm{y} i_\mathrm{ny} + d_\mathrm{S}^- i_\mathrm{nS}^- \tag{2.23}$$

with $d_i = t_i/T_0$ being the normalized application time of the ith switching vector. Since for all 7S-SSs the second and third switching vectors can be any type of switching vectors, in the above equation the subindexes $\{\mathrm{x},\, \mathrm{y}\} \in \{0, \mathrm{S}, \mathrm{M}, \mathrm{L}\}$

As shown in Table 2.2, each small vector $\boldsymbol{u}_\mathrm{S}$ drives an NP-current of the same amplitude but opposite direction that the one obtained with its single redundancy. Thereby, the condition $i_\mathrm{nS}^+ = -i_\mathrm{nS}^-$ holds for all small switching vectors, and thus, the average NP-voltage dynamic model (2.22) leads to

$$\frac{\mathrm{d}V_\mathrm{n}}{\mathrm{dt}} = \frac{1}{C_1 + C_2}(d_\mathrm{S}^+ - d_\mathrm{S}^-)i_\mathrm{nS}^+ + \frac{1}{C_1 + C_2}(d_2 i_\mathrm{n2} + d_3 i_\mathrm{n3}) \tag{2.24}$$

In consequence, for a given current vector $\boldsymbol{i}_\mathrm{abc}$, the difference $d_\mathrm{S}^+ - d_\mathrm{S}^-$ in the right-hand of the above equation can be assumed as the degree of freedom for controlling the average value of the NP-voltage. Indeed, the majority of the NP-voltage balancing schemes used in space vector modulation

(SVM) are based on manipulating the relative duration of the P-type and N-type small vectors during a switching interval [78] [79].

Therefore, the control authority over the NP-current and thus over the NP-voltage is quite limited at high modulation indices, low power factors, or low phase currents [78] [79]. Also, the control of the NP-voltage is not sufficiently effective under unsymmetrical and non-sinusoidal currents, especially when dc components are present in the phase currents [80].

2.4 Summary

This chapter presents the key role-playing by grid-connected power converters for interfacing renewable energy resources is discussed in this Chapter. Maximum harmonic current distortion allowed for grid-connected power converters are also introduced in this chapter. A brief review of control strategies for the operation of grid-connected converters has also been presented in this chapter.

Furthermore, the principle of operation and a comprehensive model of the 3L-NPC power converter is introduced in this chapter. This model allows defining the influence of the small-size switching vectors in the NP-voltage when the converter synthesizes seven-segment switching sequences. The balancing NP-voltage problem is also addressed in this chapter.

CHAPTER 3

Proposed Cascaded-Optimal Switching Sequence MPC Strategy

This chapter presents a new OSS-MPC strategy for predictive current control and predictive direct power control of grid-connected 3L-NPC converters. The proposed Cascaded-OSS-MPC (C-OSS-MPC) strategy does not require a weighting factor in the cost function to balance the dc-link capacitor voltages of the NPC-converter and optimally controls both the grid currents and the capacitor voltages even during disturbances and large step-changes in the references.

The resulting MPC strategy allows operating the converter with a predefined harmonic spectrum, relatively low switching frequency and, fast and robust dynamic responses in the whole operating range. Moreover, an efficient control algorithm is also addressed to reduce the computational burden typically observed in this kind of MPC strategies.

Besides, a detailed analysis of the optimal solution is presented. This includes the case where overmodulation is required by the control system. As a result, a low complex explicit solution is derived, which can be easily implemented in a standard digital control platform.

3.1 The Grid-Connected 3L-NPC Converter

The circuit diagram of the grid-connected 3L-NPC converter is shown in Fig. 3.1. The converter is composed of four switches and two clamped diodes per leg, producing a total of 27 three-phase switching states for the whole converter, i.e. $\boldsymbol{u}_{\rm abc}\in\mathbb{U}\triangleq\{-1,0,1\}^3$. As shown in Fig. 3.2(a), these switching states generate 19 non-redundant and 8 redundant switching vectors in the stationary $\alpha\beta$ frame, which can be obtained using the Clarke transformation (2.20) as $\boldsymbol{u}_s=\mathbf{T}_{\alpha\beta}\boldsymbol{u}_{\rm abc}\in\mathcal{U}\triangleq\mathbf{T}_{\alpha\beta}\mathbb{U}$.

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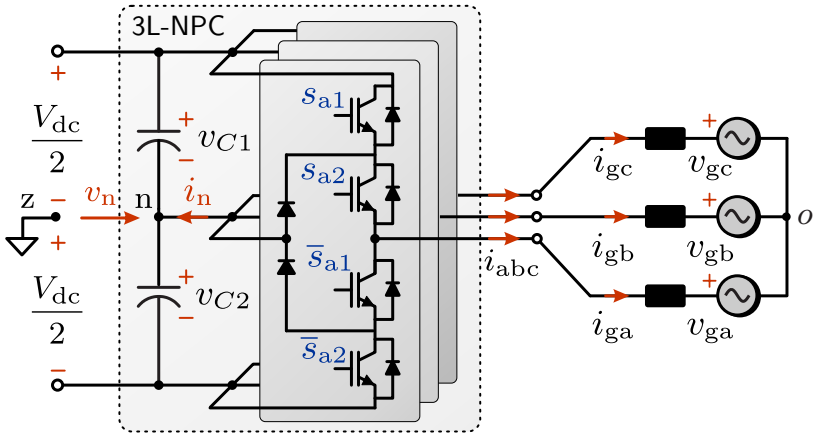

FIGURE 3.1: Grid-connected 3L-NPC converter.

To synthesise a desired inverter output voltage during a switching cycle $T_{\rm s}$, the three nearest switching vectors are typically employed in carrier-based and space vector PWM techniques [65, 76, 77]. In this context, as shown Fig. 3.2(a), the space of SVs is usually divided into 24 regions $\mathcal{R}_j\in\boldsymbol{\mathcal{R}}$, with $\boldsymbol{\mathcal{R}}\triangleq\{\mathcal{R}_1,\ldots,\mathcal{R}_{24}\}$. Formally, each region $\mathcal{R}_j$ is a convex set produced by any convex combination of a small vector $\boldsymbol{u}_{\rm S}$ and its two nearest switching vectors, i.e.,

$$\mathcal{R}_j \triangleq \left\{ \alpha_1\boldsymbol{u}_{{\rm S}i}+\alpha_2\boldsymbol{u}_{2i}+\alpha_3\boldsymbol{u}_{3i} \;\middle|\; \forall\alpha_i\geq 0 \;\wedge\; \sum_{\forall i}\alpha_i=1 \right\} \tag{3.1}$$

Furthermore, the order in which the converter applies these vectors within a sampling cycle is known as switching sequence (SS). Due to the presence of the redundancies, several switching sequences (or switching patterns) can assembly the desired output voltage. Therefore, the generation of switching sequences is considered as a degree of freedom that can be used for several purposes such as reduction of switching losses and minimal NP-voltage deviation.

Based on the above analysis, the seven-segment switching sequence (7S-SS) [76] will be adopted in this work to assembly the MPC strategy. As mentioned in the previous chapter, this switching pattern consists of four SVs which are arranged in such a way the transition between two adjacent switching states demands only one switching action. Additionally, each switching period is split

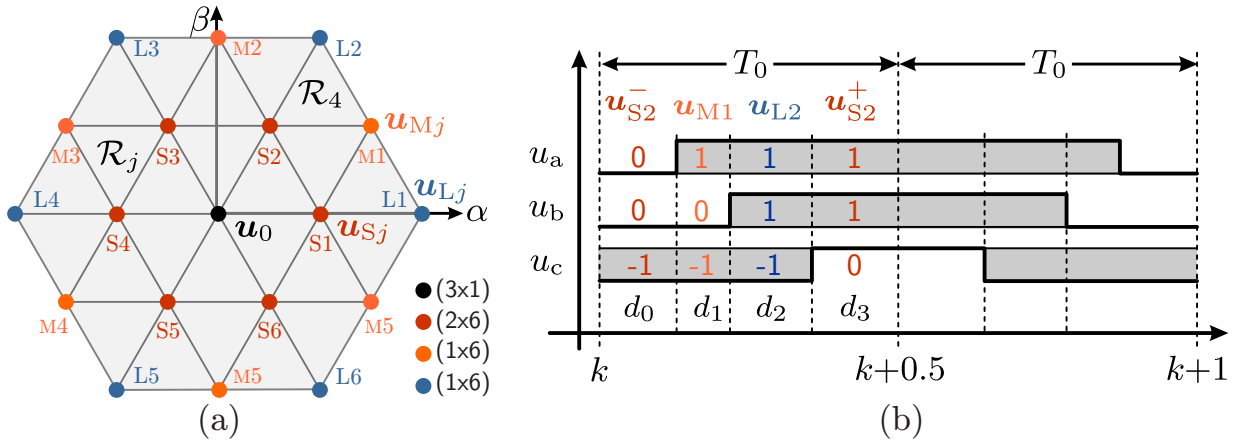

FIGURE 3.2: (a) Space of switching vectors for a 3L-NPC converter and, (b) the N-type seven-segment switching sequence for the region $\mathcal{R}_4$.

into two sub-cycles of duration $T_0{=}T_s/2$, where the disposition of the second sub-cycle being a reversal of the arrangement of the first one [76], as shown the illustrative example of Fig. 3.2(b). Furthermore, the N-type symmetric pattern will be adopted in this work in which the first sub-cycle always starts with an N-type small SV ($\boldsymbol{u}_S^-$) and ending with P-type redundancy ($\boldsymbol{u}_S^+$). Thus, the 7S-SS can be defined accordingly as

$$\boldsymbol{S} \triangleq \left\{ \boldsymbol{u}_S^-[t_0], \boldsymbol{u}_1[t_1], \boldsymbol{u}_2[t_2], \boldsymbol{u}_S^+[t_3], \boldsymbol{u}_S^+[t_3], \boldsymbol{u}_2[t_2], \boldsymbol{u}_1[t_1], \boldsymbol{u}_S^-[t_0] \right\} \tag{3.2}$$

where t_i being the application time in which the ith switching vector is synthesized by the converter, as depicted in Fig. 3.2(b).

In consequence, the primary target of the proposed control strategy is to determine the optimal switching sequence $\boldsymbol{S}^\star$ (switching sequence and application times) that allows one to minimize the tracking errors of the grid variables to be controlled meanwhile keeping the capacitor voltages balanced with acceptable ripple. As indicated in (A.1), the optimal switching sequence (OSS) is defined by the set of switching vectors $\boldsymbol{u}_{si}$ belonging to the optimal region $\mathcal{R}^*$ as well as their optimal application times t_i^*.

3.2 Proposed Cascaded-OSS MPC Strategy

One of the main challenges for the proper operation of this converter is to keep the capacitor voltages balanced with a tolerable voltage ripple [81].

Within FCS-MPC schemes, the most typical approach to balance the capacitor voltages of the 3L-NPC converter consist of minimizing a bi-objective cost function in which the NP-voltage error is directly included in the cost function [33] as:

$$J_0 = \left\| \boldsymbol{x}_{\mathrm{g}}^{*}(k{+}1) - \boldsymbol{x}_{\mathrm{g}}(k{+}1) \right\|_2^2 + \lambda_{\mathrm{n}} v_{\mathrm{n}}^2(k{+}1). \tag{3.3}$$

where $\|\boldsymbol{\xi}\|_2^2 = \boldsymbol{\xi}^{\intercal}\boldsymbol{\xi}$ is the square of the quadratic norm (euclidean norm), $\boldsymbol{x}_{\mathrm{g}}$ groups the variables of the grid to be controlled (line currents or active/reactive powers) and, λ_{n} is the weighting factor used to trade-off the control targets.

Considering this approach, the performance of the converter is sensible to the parameter λ_{n}. Indeed, there is no analytical or numerical method proposed yet to obtain optimal weighting factors and the tuning of this parameter is usually done by an empirical process which is not always straightforward mainly because it depends on the operating point and the parameters of the system [3] [82]. Furthermore, although, by theory, the multi-objective MPC problem has a unique, globally optimal solution, it does not imply optimality of each sub-performance index [52] [51].

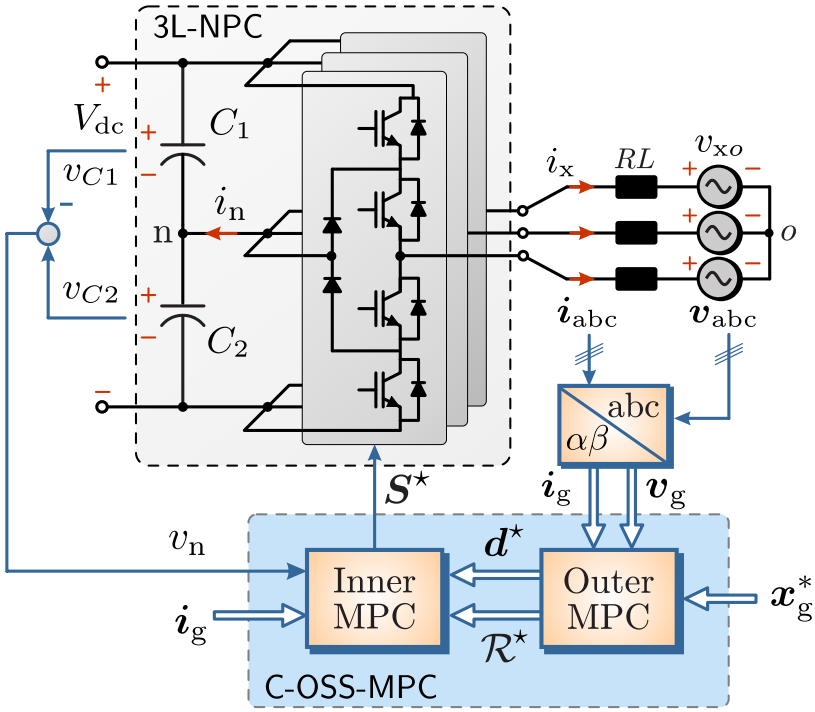

FIGURE 3.3: Grid-connected 3L-NPC converter and proposed C-OSS-MPC.

Under this perspective, the C-OSS-MPC strategy depicted in the blue block of Fig. 3.3 is proposed in this work to simultaneously control some variables of the system such as line currents or active/reactive power as well as the capacitor voltages without the use of weighting factors to trade-off the control objectives.

In the proposed control scheme depicted in Fig. 3.3, the Outer-MPC is focusing on controlling some output variables of the converter ($\boldsymbol{x}_{\mathrm{g}}$: line currents or active/reactive power) by assuming that NP-voltage is zero. The outputs of the Outer-MPC block are the optimal region $\mathcal{R}^{\star}$ and the normalized application times of the switching vectors that belong to $\mathcal{R}^{\star}$ (which are grouped in the duty cycle vector $\boldsymbol{d}^{\star}$). Next, by using the information provided by the Outer-MPC, i.e., $\mathcal{R}^{\star}$ and $\boldsymbol{d}^{\star}$, the Inner-MPC stage determines the optimal dwell-time distribution of the small switching vectors to control the NP-voltage. Consequently, the use of weighting factors is avoided with this control method and the optimal solution obtained from the Outer-MPC is not affected by the Inner-MPC stage. This comes from the fact that the sum of the application time of the small switching vector and its redundancy is not altered by the Inner-MPC.

In this chapter, the predictive Cascaded-OSS control strategy will be applied to grid-connected 3L-NPC converters for (a) the line current control and; (b) direct-power control. In consequence, two Outer-MPC strategies are introduced in the following.

3.3 The Outer MPC: OSS Model Predictive Current Control (OSS-MP-CC)

3.3.1 Continuous-Time Model

Let us consider a three-phase 3L-NPC grid-connected inverter as illustrated in Fig. 3.3. Thus, by assuming v_{n}=0, the continuous-time model for the grid current in the stationary $\alpha\beta$ frame can be expressed as

$$\frac{\mathrm{d}\boldsymbol{i}_{\mathrm{g}}}{\mathrm{d}t} = -\frac{R}{L}\boldsymbol{i}_{\mathrm{g}} + \frac{1}{L}\left(\frac{1}{2}V_{\mathrm{dc}}\boldsymbol{u}_s - \boldsymbol{v}_{\mathrm{g}}\right) \tag{3.4}$$

with $\boldsymbol{v}_{\mathrm{g}}=\begin{bmatrix} v_{\mathrm{g}\alpha} & v_{\mathrm{g}\beta}\end{bmatrix}^{\intercal}$ the grid voltage vector.

For this case, the variable to be controlled is the grid current vector, thus $\boldsymbol{x}_{\mathrm{g}} = \boldsymbol{i}_{\mathrm{g}}$, and the state-space continuous-time model (3.4) can be written as

$$\frac{\mathrm{d}\boldsymbol{x}_{\mathrm{g}}}{\mathrm{d}t} = a_1\boldsymbol{x}_{\mathrm{g}} + a_2\boldsymbol{v}_{\mathrm{g}} + b_1\boldsymbol{u}_s \tag{3.5}$$

where $a_1 = -R/L$, $a_2 = -1/L$ and, $b_1 = V_{\mathrm{dc}}/2L$.

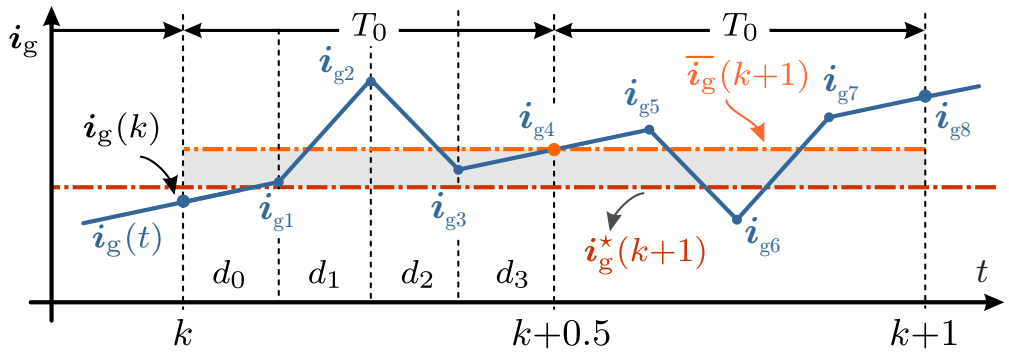

FIGURE 3.4: Predicted system trajectory for a 7S-SS.

3.3.2 Discrete-Time Model: the Average Trajectory

Commonly in FCS-MPC strategies, the optimal control action is derived from the minimization of a cost function that compares the reference and the prediction of the variables to be controlled at the end of the sampling period. In a different manner, this work proposes using the prediction of the average trajectory over the whole switching cycle T_{s} when the converter synthesizes a 7S-SS as per (A.1). This approach allows reducing the average tracking error and consequently the overall controlled system performance is improved.

For a simple calculation of the average trajectory of the grid current, let us assume a switching cycle sufficiently smaller than the time constant of the system (3.4), i.e., $T_{\mathrm{s}} \ll L/R$. Accordingly, when the converter applies a 7S-SS, the instantaneous evolution of $\boldsymbol{i}_{\mathrm{g}}$ during the switching period can be considered as a piecewise linear function of the time, as illustrated in Fig. 3.4. According to (3.5), the ith subinterval slope can be expressed in terms of the switching vector that converter applies during the whole subinterval as

$$\left.\frac{\mathrm{d}\boldsymbol{x}_{\mathrm{g}}}{\mathrm{d}t}\right|_i = a_1\boldsymbol{x}_{\mathrm{g}(i)} + a_2\boldsymbol{v}_{\mathrm{g}(i)} + b_1\boldsymbol{u}_{s(i)} \tag{3.6}$$

Thus, the instantaneous evolution of $\boldsymbol{x}_{\mathrm{g}}$ can be computed by employing the one-step Euler method as

$$\boldsymbol{x}_{g(i+1)} = \boldsymbol{x}_{\mathrm{g}(i)} + \left.\frac{\mathrm{d}\boldsymbol{x}_{\mathrm{g}}}{\mathrm{d}t}\right|_i T_0\, d_i \tag{3.7}$$

where $d_i{=}t_i/T_0$ is the normalized application time (or duty cycle) of the ith switching vector $\boldsymbol{u}_{si}$ that belongs to any 7S-SS.

Furthermore, by taking into account the symmetrical nature of the 7S-SS, it can be demonstrated (see Appendix) that the average trajectory of the grid current corresponds to its instantaneous value at the end of the sub-cycle, i.e., $\overline{\boldsymbol{i}_{\mathrm{g}}}(k{+}1) = \boldsymbol{i}_{\mathrm{g4}}$, as depicted in Fig. 3.4. Therefore, when the con-

verter applies a 7S-SS, the predicted average trajectory is given by

$$\overline{\boldsymbol{x}}_{\mathrm{g}}(k{+}1) = \boldsymbol{x}_{\mathrm{g}}(k) + T_0 \sum_{i=0}^{3} \left.\frac{\mathrm{d}\boldsymbol{x}_{\mathrm{g}}}{\mathrm{d}t}\right|_i d_i \tag{3.8}$$

It is worth to highlight that, as shown in (3.6) and (3.8), the average trajectory depends on the duty cycles in a non-linear manner. To simplify the analysis, the ith subinterval slope (3.6) is approximated by using the sampled values for the current and voltage grid vectors as

$$\left.\frac{\mathrm{d}\boldsymbol{x}_{\mathrm{g}}}{\mathrm{d}t}\right|_i \approx a_1 \boldsymbol{x}_{\mathrm{g}}(k) + a_2 \boldsymbol{v}_{\mathrm{g}}(k) + b_1 \boldsymbol{u}_{si}.$$

Under this perspective, it is assumed that the subinterval slopes do not depend on the inter-sampling current trajectory. Therefore, the prediction of the average trajectory (3.8) can be expressed as

$$\overline{\boldsymbol{x}}_{\mathrm{g}}(k{+}1) = \alpha_1 \boldsymbol{x}_{\mathrm{g}}(k) + \alpha_2 \boldsymbol{v}_{\mathrm{g}}(k) + \beta \sum_{i=0}^{3} \boldsymbol{u}_{si} d_i \tag{3.9}$$

with $\alpha_1{=}1{-}T_0\frac{R}{L}$, $\alpha_2{=}-\frac{T_0}{L}$, and $\beta{=}\frac{1}{2}V_{\mathrm{dc}}\frac{T_0}{L}$.

Finally, on the grounds that for any N-type seven-segment switching sequence we have that $\boldsymbol{u}_{s0} = \boldsymbol{u}_{\mathrm{S}}^{-}$ and $\boldsymbol{u}_{s3} = \boldsymbol{u}_{\mathrm{S}}^{+}$. Therefore, the following linear representation of the average trajectory can be stated:

$$\overline{\boldsymbol{x}}_{\mathrm{g}}(k{+}1) = \alpha_1 \boldsymbol{x}_{\mathrm{g}}(k) + \alpha_2 \boldsymbol{v}_{\mathrm{g}}(k) + \beta \boldsymbol{U}(k)\boldsymbol{d}(k) \tag{3.10}$$

where the duty cycle vector and switching matrix are introduced as follows:

$$\boldsymbol{d}(k) \triangleq \begin{bmatrix} d_{\mathrm{S}}(k) & d_1(k) & d_2(k) \end{bmatrix}^{\mathsf{T}} \in \mathbb{D} \triangleq [0,1]^3, \tag{3.11}$$

$$\boldsymbol{U}(k) \triangleq \begin{bmatrix} \boldsymbol{u}_{\mathrm{S}}(k) & \boldsymbol{u}_1(k) & \boldsymbol{u}_2(k) \end{bmatrix}, \tag{3.12}$$

with $d_{\mathrm{S}}{=}d_0{+}d_3$, the sum of the application times of the small switching vectors.

For the sake of simplicity, hereinafter $\overline{\boldsymbol{x}_{\mathrm{g}}}(k{+}1)$ will be denoted as $\boldsymbol{x}_{\mathrm{g}}(k{+}1)$; and consequently, (3.10) will be the discrete-time model for the predictive OSS current control strategy.

As shown in (3.10), the degrees of freedom to get the control targets are the duty cycles. It follows that, in order to calculate the optimal dwell times, a cost function measuring somehow the gap between $\boldsymbol{x}_{\mathrm{g}}(k{+}1)$ and its reference $\boldsymbol{x}_{\mathrm{g}}(k{+}1)$ should be defined.

3.3.3 Optimal Control Problem for OSS-MP-CC

To obtain the optimal duty cycles, the following quadratic cost function is introduced

$$J_{\mathrm{i}}(\boldsymbol{d}(k)) = \big\|\boldsymbol{i}_{\mathrm{g}}(k{+}1){-}\boldsymbol{i}_{\mathrm{g}}^{\star}(k{+}1)\big\|_2^2 + \lambda_{\mathrm{u}}\big\|\boldsymbol{u}(k){-}\boldsymbol{u}_{\mathrm{ss}}(k)\big\|_2^2 \tag{3.13}$$

which is a suitable choice to trade the grid current tracking error versus control input effort, where

$$\boldsymbol{u}(k) = \boldsymbol{U}(k)\boldsymbol{d}(k) \in \mathbb{V} \triangleq \mathbf{T}_{\alpha\beta}\mathbb{D} \tag{3.14}$$

is the average switching vector applied by the converter within a switching cycle and, $\boldsymbol{u}_{\mathrm{ss}}(k)$ is the required input to maintain the grid current vector at the desired steady-state operating conditions [39]. Thus, according to (3.4), it can be obtained as:

$$\boldsymbol{u}_{\mathrm{ss}}(k) = \frac{2}{V_{\mathrm{dc}}}\Big(\big(\mathbf{J}\omega_{\mathrm{g}}L + \mathbf{I}_2 R\big)\,\boldsymbol{i}_{\mathrm{g}}^{\star}(k{+}1) + \boldsymbol{v}_{\mathrm{g}}(k)\Big) \tag{3.15}$$

Accordingly, the tuning parameter λ_{u} can be used to regulate the closed-loop bandwidth of the controller. Therefore, if λ_{u} is too small (≈ 0), then the first term in (3.13) becomes predominant; and hence, the controller will have a structure similar to a multi-variable deadbeat controller. Conversely, if λ_{u} is too large, the optimal solution tends to $\boldsymbol{u}_{\mathrm{ss}}(k)$ which is equivalent to operate in an open-loop fashion [29]. Indeed, by replacing the prediction of the average trajectory (3.10) into (3.13), the cost function can be finally expressed as:

$$J_{\mathrm{i}}(\boldsymbol{d}(k)) = \lambda_{\mathrm{i}}\big\|\boldsymbol{U}\boldsymbol{d}(k) - \boldsymbol{u}_{\mathrm{db}}(k)\big\|_2^2 {+} \lambda_{\mathrm{u}}\big\|\boldsymbol{U}\boldsymbol{d}(k) - \boldsymbol{u}_{\mathrm{ss}}(k)\big\|_2^2, \tag{3.16}$$

where

$$\boldsymbol{u}_{\mathrm{db}} {=} \frac{1}{\beta}\big(\boldsymbol{i}_{\mathrm{g}}^{\star}(k{+}1) - \alpha_1\boldsymbol{i}_{\mathrm{g}}(k) - \alpha_2\boldsymbol{v}_{\mathrm{g}}(k)\big). \tag{3.17}$$

is the deadbeat control input and

$$\lambda_{\mathrm{i}} = \beta^2 {=} \frac{V_{\mathrm{dc}}^2 T_0^2}{4L^2} \tag{3.18}$$

is a non-negative scalar.

On the other hand, the duty cycle vector of any 7S-SS has to satisfy $\mathbb{1}^{\intercal}\boldsymbol{d}(k) = 1$ and $\boldsymbol{d}(k) \in \mathbb{D}$. Therefore, the optimal switching sequence (OSS) is obtained by solving, at each sampling instant k, the following constrained optimization problem:

$$\{\boldsymbol{U}^{\star}, \boldsymbol{d}^{\star}\} = \arg\min_{\boldsymbol{U}_j}\Big\{\min_{\boldsymbol{d}_j}\; J_{\mathrm{i}}(\boldsymbol{d}_j, \boldsymbol{U}_j)\Big\} \tag{3.19a}$$

$$\text{s.t.}\;\; \mathbb{1}^{\intercal}\boldsymbol{d}_j = 1 \tag{3.19b}$$

$$\boldsymbol{d}_j \geq 0. \tag{3.19c}$$

Notice that the constrained optimization problem (COP) considers two optimization stages. Firstly, in the internal optimization, for each switching sequence candidate $\boldsymbol{U}_j$, a local minima solution $\boldsymbol{d}_j$ can be computed. According to its structure, the internal optimization is known as a box-constrained least-square (BCLS) problem [52]. On the other hand, in the external optimization stage, once the duty cycles are obtained, the cost function (3.13) can be evaluated for each pair $\{\boldsymbol{U}_j, \boldsymbol{d}_j\}$. Finally, the pair that provides the minimum cost value defines the OSS by using (A.1).

Typically, the global optimum for this kind of FCS-MPC strategies is obtained by implementing an enumerate algorithm in which the internal optimization problem in (3.19) is solved for every region in which the space of SVs has been divided [44–50]. In the case of 3L-NPC converters this implies a searching over the set $\boldsymbol{\mathcal{R}}=\{\mathcal{R}_1, \ldots, \mathcal{R}_{24}\}$. Alternatively, a more efficient optimizer will be introduced in section 3.4, which takes advantage of some property of (3.19) to reduce the computational burden of the controller.

3.4 Optimization Process for the Outer-MPC

Because the constrained optimization problem (3.19) should be solved for every one of the 24 regions at each sampling period, a suitable strategy to efficiently find its optimal solution is introduced in this section. To do this, it is proposed first to compute the solution of the relaxed problem and then, to apply a simple methodology to fulfil the non-negative constraint; and hence, to obtain the OSS.

3.4.1 Relaxed solution

In the relaxed problem, the non-negative constraint over the duty cycle is ignored [inequality $\boldsymbol{d}(k)\geq 0$ in (3.19c)]. In consequence, the relaxed solution for each 7S-SS candidate, denoted as $\boldsymbol{d}_{\mathrm{r}j}$, has to solve the following constrained least-square (CLS) problem, i.e,

$$\begin{aligned} \boldsymbol{d}_{\mathrm{r}j} = \arg\min_{\boldsymbol{d}_j} \;\; & \lambda_{\mathrm{i}} \left\| \boldsymbol{U}_j \boldsymbol{d}_j - \boldsymbol{u}_{\mathrm{db}} \right\|_2^2 + \lambda_{\mathrm{u}} \left\| \boldsymbol{U}_j \boldsymbol{d}_j - \boldsymbol{u}_{\mathrm{ss}} \right\|^2 \\ \text{s. t.} \;\; & \mathbb{1}^{\intercal} \boldsymbol{d}_j = 1. \end{aligned} \tag{3.20}$$

Thereby, using the Lagrange method [52], for each switching sequence candidate, the solution to this bi-objective CLS problem can be obtained by solving the following linear system of 4 equations:

$$\begin{bmatrix} (\lambda_{\mathrm{i}} + \lambda_{\mathrm{u}}) \boldsymbol{U}_j^{\intercal} \boldsymbol{U}_j & \mathbb{1} \\ \mathbb{1}^{\intercal} & 0 \end{bmatrix} \begin{bmatrix} \boldsymbol{d}_{\mathrm{r}j} \\ \nu \end{bmatrix} = \begin{bmatrix} \boldsymbol{U}_j^{\intercal} (\lambda_{\mathrm{i}} \boldsymbol{u}_{\mathrm{db}} + \lambda_{\mathrm{u}} \boldsymbol{u}_{\mathrm{ss}}) \\ 1 \end{bmatrix} \tag{3.21}$$

Furthermore, because of the matrix dimensions involved in (3.21), i.e., the dimensions of $\boldsymbol{U}$ and $\boldsymbol{d}_{\mathrm{r}}$ are (2×3) and (3×1), respectively, the conditions $\nabla J_{\mathrm{i}}(\boldsymbol{d}_{\mathrm{r}})=0$ and $\mathbb{1}^{\intercal}\boldsymbol{d}_{\mathrm{r}}=1$ are satisfied

simultaneously. Thus, the Lagrange multiplier must be $\nu = 0$; and consequently, the relaxed solution associated to the jth region (which not necessarily fulfils $\boldsymbol{d}_{\mathrm{r}} \geq 0$) can be directly computed according to

$$\boldsymbol{d}_{\mathrm{r}j} = \begin{bmatrix} \boldsymbol{U}_j \\ \mathbb{1}^{\intercal} \end{bmatrix}^{-1} \begin{bmatrix} \boldsymbol{u}_{\mathrm{uc}} \\ 1 \end{bmatrix}, \tag{3.22}$$

with $\boldsymbol{u}_{\mathrm{uc}}$ the unconstrained average switching vector given by

$$\boldsymbol{u}_{\mathrm{uc}}(k) = \begin{bmatrix} u_{\mathrm{uc}\alpha} \\ u_{\mathrm{uc}\beta} \end{bmatrix} = \frac{1}{\lambda_{\mathrm{i}} + \lambda_{\mathrm{u}}} \Big(\lambda_{\mathrm{i}} \boldsymbol{u}_{\mathrm{db}}(k) + \lambda_{\mathrm{u}} \boldsymbol{u}_{\mathrm{eq}}(k) \Big) \tag{3.23}$$

It is worth to bear on mind that (3.22) is guaranteed since the (3×3) stacked matrix $[\boldsymbol{U}^{\intercal}\ \mathbb{1}]^{\intercal}$ has linearly independent columns for all regions. Finally, its explicit form is given by

$$\begin{bmatrix} d_{\mathrm{rS}} \\ d_{\mathrm{r1}} \\ d_{\mathrm{r2}} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} u_{1\beta} - u_{2\beta} & u_{2\alpha} - u_{1\alpha} & \boldsymbol{u}_2 \times \boldsymbol{u}_2 \\ u_{2\beta} - u_{\mathrm{S}\beta} & u_{\mathrm{S}\alpha} - u_{2\alpha} & \boldsymbol{u}_2 \times \boldsymbol{u}_{\mathrm{S}} \\ u_{\mathrm{S}\beta} - u_{1\beta} & u_{1\alpha} - u_{\mathrm{S}\alpha} & \boldsymbol{u}_{\mathrm{S}} \times \boldsymbol{u}_1 \end{bmatrix} \begin{bmatrix} u_{\mathrm{r}\alpha} \\ u_{\mathrm{r}\beta} \\ 1 \end{bmatrix} \tag{3.24}$$

where

$$\Delta = \boldsymbol{u}_{\mathrm{S}} \times \boldsymbol{u}_1 + \boldsymbol{u}_2 \times \boldsymbol{u}_{\mathrm{S}} + \boldsymbol{u}_1 \times \boldsymbol{u}_2,$$

and $\boldsymbol{u}_x \times \boldsymbol{u}_y = u_{x\alpha} u_{y\beta} - u_{x\beta} u_{y\alpha}$ denotes the cross product.

3.4.2 Optimal Solution

As described in (3.22), every one of the local solutions $\boldsymbol{d}_{\mathrm{r}j}$ defines a unique point onto the $\alpha\beta$-plane by means of using the mapping $\boldsymbol{u}_{\mathrm{uc}} = \boldsymbol{U}_j \boldsymbol{d}_{\mathrm{r}j}$. This point is, indeed, the unconstrained average switching vector given in (3.23).

Under this perspective, the cost function (3.16) is rewritten in terms of the unconstrained average switching vector as

$$J(\boldsymbol{u}) = (\lambda_{\mathrm{i}} + \lambda_{\mathrm{u}})(\boldsymbol{u} - \boldsymbol{u}_{\mathrm{uc}})^{\intercal}(\boldsymbol{u} - \boldsymbol{u}_{\mathrm{uc}}) + c, \tag{3.25}$$

where $c = c(k)$ does not depend on decision variable $\boldsymbol{u}$.

It is worth to note here that the level set of (3.25) describe spheres centered in $\boldsymbol{u}_{\mathrm{uc}}(k)$ as illustrated in Fig. 3.5. Consequently, the optimal average switching vector (OASV) $\boldsymbol{u}^*$ corresponds to the point on the $\alpha\beta$ plane closest to $\boldsymbol{u}_{\mathrm{uc}}$.

3.4.2.a Direct Solution

Under the assumption that $\boldsymbol{u}_{\mathrm{uc}}(k)$ falls within the control region, i.e., $\boldsymbol{u}_{\mathrm{uc}}(k) \in \mathbb{V}$ (hexagon shown in Fig. 3.5(a)), then there exists only one region $\mathcal{R}^{\star}$ able to generate $\boldsymbol{u}_{\mathrm{uc}}$ through a convex combination

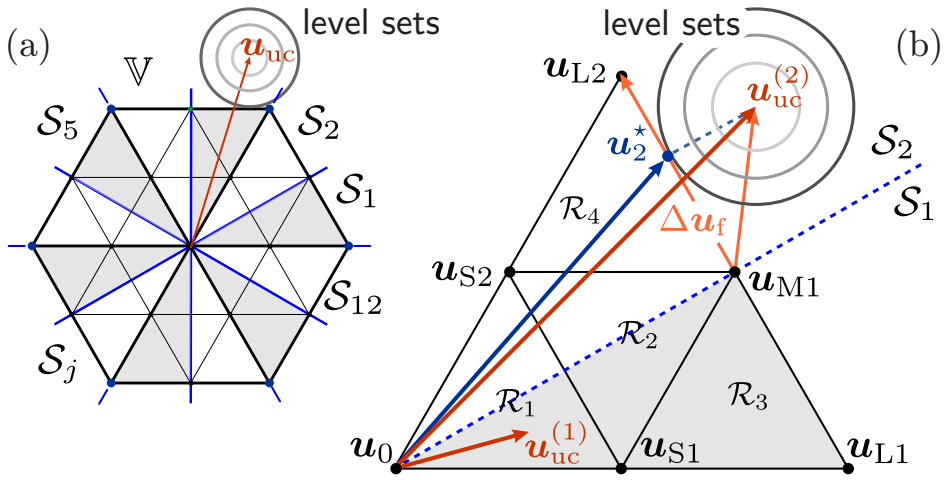

FIGURE 3.5: The relation between the unconstrained solution and the optimal average switching vector; (a) partition of the control region and; (b) illustrative examples.

of its three switching vectors. According to (3.1), only one among all the local solutions [which are computed using (3.24)] satisfies the constrain $\boldsymbol{d}(k)\geq 0$; and hence, it will be the global optimal solution $\boldsymbol{d}^{\star}$.

Therefore, the only relaxed solution satisfying the constraint $\boldsymbol{d}_{\rm r}\geq 0$ is directly related to the region in which $\boldsymbol{u}_{\rm uc}$ is located in the $\alpha\beta$-plane. Under this perspective, if the $\alpha\beta$ plane is divided into 12 sectors $\mathcal{S}_j\in\boldsymbol{\mathcal{S}}=\{\mathcal{S}_1,\ldots,\mathcal{S}_{12}\}$, as depicted in Fig. 3.5(a), the OASV must be into one of the three regions intersecting to the optimal sector $\mathcal{S}_{j_{\rm op}}$ where $j_{\rm op}$ is computed from $\boldsymbol{u}_{\rm uc}$ as

$$j_{\rm op} = \text{floor}\left\{\frac{6}{\pi}\tan^{-1}\left(\frac{u_{\rm uc\beta}}{u_{\rm uc\alpha}}\right)\right\} + 1 \tag{3.26}$$

Hence, by using the angular position of $\boldsymbol{u}_{\rm uc}$, the conventional enumeration algorithm for which the closed-form solution (3.22) is evaluated is certainly reduced from 24 to only 3. Moreover, within the set of three 7S-SS candidates, only one satisfies the constraint (3.19c). Thus, the global optimal normalized times can be found by directly evaluating the non-negativity condition of the three relaxed solutions computed by using (3.22) (one each per a region). In this regard, the cost function evaluation to obtain the optimal region is also avoided in this work, which certainly reduces the computational burden of the controller.

In Fig. 3.5(b), an illustrative example is shown for $\boldsymbol{u}_{\rm uc}^{(1)}$. Here, the relaxed solution computed from (3.22) as

$$\boldsymbol{d}_{\rm r1} = \begin{bmatrix} \boldsymbol{u}_{\rm S1} & \boldsymbol{u}_{\rm S2} & \boldsymbol{u}_0 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} \boldsymbol{u}_{\rm uc}^{(1)} \\ 1 \end{bmatrix}, \tag{3.27}$$

is necessarily non-negative; and consequently, it will be the global optimum normalized times.

It is worth to emphasize that the partition of the control region addressed in this section [shown in Fig. 3.5(a)] allows to directly determine the dominant small size switching vector for the region 1 or 2 with which the 7S-SS (A.1) should be implemented (see section 2.3.4). In this regard and considering the example illustrated in Fig. 3.5(b), to synthesize $\boldsymbol{u}_{\rm uc}^{(1)}$, the 7S-SS is executed by using $\boldsymbol{u}_{\rm S1}$ as the dominant small vector instead of $\boldsymbol{u}_{\rm S2}$. In consequence, the N-type 7S-SS for this example is given by

$$\boldsymbol{S}=\Big\{\boldsymbol{u}_{\rm S1}^{-}[d_0],\boldsymbol{u}_{\rm S2}^{-}[d_1],\boldsymbol{u}_0[d_2],\boldsymbol{u}_{\rm S1}^{+}[d_3],\boldsymbol{u}_{\rm S1}^{+}[d_3],\boldsymbol{u}_0[d_2],\boldsymbol{u}_{\rm S2}^{-}[d_1],\boldsymbol{u}_{\rm S1}^{-}[d_0]\Big\}$$

3.4.2.b Overmodulation

If conversely, $\boldsymbol{u}_{\rm uc}$ falls out of the control region, none of the 24 local solutions is non-negative. In this case, which commonly occurs during transient processes, the resulting OASV necessarily is on the perimeter of the hexagon shown in Fig. 3.5(a). In this regard, the inner optimization problem in (3.19) is solved for the outer region that belongs to $\mathcal{S}_{j_{\rm op}}$ by forcing that $d_{\rm S}=0$ (duty cycle of the small SV must be zero). Therefore, the optimal normalized times for the medium- and large- size SVs are computed as:

$$\begin{aligned}\mu_{\rm L}^{\star}&=\operatorname{mid}\left\{0,\ \frac{(\boldsymbol{u}_{\rm L}-\boldsymbol{u}_{\rm M})^{\intercal}\big(\boldsymbol{u}_{\rm uc}(k)-\boldsymbol{u}_{\rm M}\big)}{\|\Delta\boldsymbol{u}_{\rm f}\|^2},\ 1\right\}\\ \mu_{\rm M}^{\star}&=1-\mu_{\rm L}^{\star},\end{aligned}\tag{3.28}$$

where $\operatorname{mid}\{\cdot\}$ defines the component-wise median and, $\|\Delta\boldsymbol{u}_{\rm f}\|^2=(2/3)^2$ for all regions. It follows that (3.28) leads to the orthogonal projection of $\boldsymbol{u}_{\rm uc}(k)$ to the hexagon's frontier. An illustrative example is shown in Fig. 3.5, in which $\boldsymbol{u}_{\rm uc}^{(2)}$ is projected to border of the hexagon resulting in the blue-line optimal vector $\boldsymbol{u}_2^{\star}$. Notice that for all regions, $\|\Delta\boldsymbol{u}_{\rm f}\|^2=(2/3)^2$.

3.5 Inner-MPC: Capacitor Voltage Balancing Strategy

Regarding the proposed C-OSS-MPC strategy depicted in Fig. 3.3, as mentioned earlier, the Inner-MPC controller is focused on controlling the capacitor voltages by making use of the optimal region $\mathcal{R}^{\star}$ and the normalized application times of its switching vectors $\boldsymbol{d}^{\star}=[d_{\rm S}^{\star}\ d_2^{\star}\ d_3^{\star}]\in\mathbb{D}$. They are provided by the Outer-MPC stage of the C-OSS-MPC strategy, as it was explained in the previous section.

As described in section 2.3.5, the dwell-time distribution of the small-size vectors allows the controller to regulate the NP-voltage [76, 78]. Hence, once the OSS is provided by the Outer-MPC stage, the Inner-MPC block shown in Fig. 3.3 divides, in an optimal manner, the duty cycle of the small vectors $d_{\rm S}^{\star}=d_1+d_4$ by introducing a distribution factor ϑ. Thereby, the duty cycle for the

small vector and its redundancy can be parametrized as

$$d_{\mathrm{S}}^{+} = \vartheta d_{\mathrm{S}}^{\star} \qquad ; \qquad d_{\mathrm{S}}^{-} = (1-\vartheta) d_{\mathrm{S}}^{\star} \tag{3.29}$$

To optimally compute this parameter, the following optimization problem is proposed in this work:

$$\min_{\vartheta} \ \left(\overline{v}_{\mathrm{n}}(k{+}1)(\vartheta) - v_{\mathrm{n}}^{\star}\right)^2 \tag{3.30a}$$

$$\text{s.t.} \ \ \vartheta \in [0,\, 1] \tag{3.30b}$$

where $\overline{v}_{\mathrm{n}}(k{+}1)$ is the predicted average NP-voltage when the converter applies any 7S-SS. It follows that, by replacing (3.29) into (2.24), this voltage can be determined as

$$\overline{v}_{\mathrm{n}}(k{+}1){=}v_{\mathrm{n}}(k) + \frac{T_0}{C_1 + C_2}\left(i_{\mathrm{n}2}^{\star} d_2^{\star} + i_{\mathrm{n}3}^{\star} d_3^{\star} + (2\vartheta - 1) i_{\mathrm{n}\mathrm{S}}^{\star} d_{\mathrm{S}}^{\star}\right) \tag{3.31}$$

where $i_{\mathrm{n}i}^{\star}$ is the NP-current associated to the i-th switching vector of the optimal region $\mathcal{R}^{\star}$. According to (2.18), it is computed as follows

$$i_{\mathrm{n}(i)} = |u_{\mathrm{a}}(\boldsymbol{u}_{si})| i_{\mathrm{a}} + |u_{\mathrm{b}}(\boldsymbol{u}_{si})| i_{\mathrm{b}} + |u_{\mathrm{c}}(\boldsymbol{u}_{si})| i_{\mathrm{c}} \tag{3.32}$$

Therefore, the unconstrained solution to the inner-MPC is given by

$$\vartheta_{\mathrm{unc}} = \frac{1}{2}\left(1 - \frac{v_{\mathrm{n}}(k) - v_{\mathrm{n}}^{\star} + x_{\mathrm{c}} T_0 (i_{\mathrm{n}2}^{\star} d_2^{\star} + i_{\mathrm{n}3}^{\star} d_3^{\star})}{x_{\mathrm{c}} T_0 i_{\mathrm{n}\mathrm{S}}^{\star} d_{\mathrm{S}}^{\star}}\right), \tag{3.33}$$

and the optimal distribution for the small switching vectors can be directly computed as

$$\vartheta^{\star} = \mathrm{mid}\{0,\, \vartheta_{\mathrm{unc}},\, 1\} \tag{3.34}$$

where $\mathrm{mid}\{\cdot\}$ defines the component-wise median.

It is important to highlight here that the optimal distribution factor for the small-size switching vectors given in (3.34) does not influence the optimal switching vector provided by the outer optimization stage. This feature comes from the fact that the sum of the P- and N-type small vector application times is not affected by the Inner-MPC controller.

3.6 Optimized Controller Algorithm

The flow diagram of the Cascaded-OSS-MP-CC for 3L-NPC converter is shown in Fig. 3.6. The algorithm starts computing $\boldsymbol{u}_{\mathrm{ss}}(k)$ and $\boldsymbol{u}_{\mathrm{db}}(k)$ using, respectively, (3.15) and (3.17) to determine

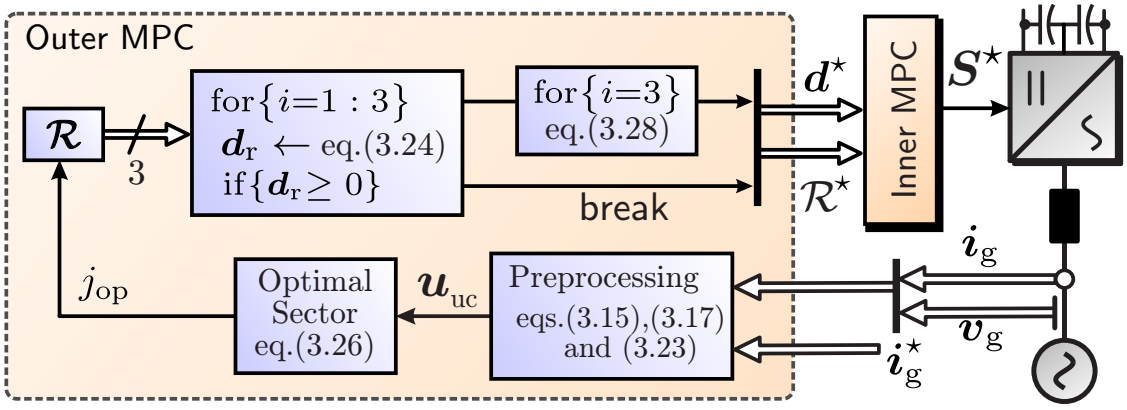

FIGURE 3.6: C-OSS-MPC with the optimizer for the Outer-MPC.

the unconstrained switching vector $\boldsymbol{u}_\mathrm{uc}(k)$ with (3.23). Then, the optimal sector in which $\boldsymbol{u}_\mathrm{uc}(k)$ is located is established by employing (3.26). Once the optimal sector has been identified, the relaxed solution is sequentially computed for the three regions inside of $\mathcal{S}_{j\mathrm{op}}$. If during this process the non-negative condition of the ith relaxed solution is satisfied, the algorithm breaks, providing, therefore, the optimal region and duty cycle ($\mathcal{R}^\star$ and $\boldsymbol{d}^\star$, respectively). On the contrary case, one additional step is carried out for the outer region ($i = 3$). Here, the duty cycle for the large and medium switching vectors are respectively computed by employing (3.28). It is worth noting here that using this algorithm, the number of potential regions to be evaluated is reduced from 24 to 3.

Finally, in the Inner-MPC stage, the duty-cycle of the small vectors are optimally distributed according to (3.29) by using the optimal parameter $\vartheta^\star$ given in (3.34). Then, the resulting optimal 7S-SS, $\boldsymbol{S}^\star$, is sent to the suitable modulator.

3.6.1 Weighting Factor Design

To design the parameter λ, the relaxed switching vector $\boldsymbol{u}_\mathrm{u}c$ can be used. As shown in (3.23), $\boldsymbol{u}_\mathrm{r}$ is the weighted sum between the deadbeat $\boldsymbol{u}_\mathrm{db}$ and steady-state $\boldsymbol{u}_\mathrm{ss}$ control inputs. It follows that by chosen $\lambda_0 = \beta^2$, the resulting OASV (which is the feasible vector closest to $\boldsymbol{u}_\mathrm{uc}$) will put the same priority to both control targets. Thus, by starting from this setting of the weighting factor, i.e.,

$$\lambda_\mathrm{u} = \lambda_0 = \frac{V_\mathrm{dc}^2 T_0^2}{4L^2}, \tag{3.35}$$

the weighting factor can be reduced or increased in order to manipulate the closed-loop dynamic response with suitable noise rejection. It is worth to highlight that both control targets drive the controlled system in the same direction during steady-state operating conditions, which simplifies the weighting factor design process. Indeed, the deadbeat control input given in (3.17) can be

rewritten as follows:

$$\boldsymbol{u}_{\mathrm{db}}=\frac{2}{V_{\mathrm{dc}}}\left(L\frac{\boldsymbol{i}_{\mathrm{g}}^{\star}(k+1)+\boldsymbol{i}_{\mathrm{g}}(k)}{T_0}+R\boldsymbol{i}_{\mathrm{g}}(k)-\boldsymbol{v}_{\mathrm{g}}(k)\right). \tag{3.36}$$

During steady-state operating conditions, it is assumed that $\boldsymbol{i}_{\mathrm{g}}(k)=\boldsymbol{i}_{\mathrm{g}}^{\star}(k)$. Therefore, the first term in the right-hand of (3.36), i.e., $\frac{\boldsymbol{i}_{\mathrm{g}}^{\star}(k+1)-\boldsymbol{i}_{\mathrm{g}}(k)}{T_0}$, can be considered as the time derivative of $\boldsymbol{i}_{\mathrm{g}}^{\star}(k+1)$. It follows that the dead-beat control input can be approximate in steady-state according to

$$\boldsymbol{u}_{\mathrm{db}}\approx\frac{2}{V_{\mathrm{dc}}}\left(\mathbf{J}\omega_{\mathrm{g}}L\boldsymbol{i}_{\mathrm{g}}^{\star}(k+1)+R\boldsymbol{i}_{\mathrm{g}}(k)+\boldsymbol{v}_{\mathrm{g}}(k)\right), \tag{3.37}$$

which certainly is very similar to the steady-state control input defined in (3.15). This fact demonstrates that, during steady-state operating conditions, both control targets drive the controlled system to approximately the same point.

3.7 Outer MPC: OSS Model Predictive Direct Power Control (OSS-MP-DPC)

Direct Power Control (DPC) is a popular scheme for the control of grid-connected power converters. DPC directly controls the instantaneous active and reactive power by selecting the switching states of the converter without using any inner-loop current regulators [57–64]. As described in [57], in the standard approach, the optimal switching actions are obtained by utilizing a lookup table and hysteresis bounds.

DPC using OSS-MPC was firstly introduced for two-level grid-connected converters in [60]. In this work, the control strategy directly selects the SVs to be applied by using the angular position of the grid voltage vector. It computes the optimal commutation instants by minimizing a quadratic cost function focusing on the active and reactive tracking errors. This provides a fixed switching frequency and good dynamic response. Nonetheless, its performance can be affected by an incorrect voltage sequence selection. To overcome this drawback, an algorithm to optimally obtain the sector in which the inverter voltage is located is proposed in [62]. Here, the algorithm computes the optimal commutation instants for each of the six sectors by employing a closed-form solution including a saturation strategy to obtain feasible and non-negative solutions. This provides six local optimal times and their associated cost values. Similar to FCS-MPC approach, the global switching instants applied by this P-DPC strategy are those minimizing the power cost function. Experimental results show the desired fixed switching behavior in steady-state condition and the intrinsic fast dynamic response provided by MPC during transients. However, sub-optimal commutation instants are provided by these controllers during transient operating conditions, in which the non-negative constraint is violated for every local solution. Besides, the dc-link capacitor voltage

balancing problem has not been addressed in these publications.

3.7.1 Continuous-Time Model

As was discussed earlier, the proposed C-OSS MPC strategy will also be implemented for direct power control. In this regard, the dynamic model for the active and reactive power is derived first.

According to the instantaneous power theory [67], the active and reactive powers injected into the grid, p_{g} and q_{g}, can be grouped into the apparent power vector $\boldsymbol{x}_p = \begin{bmatrix} p_{\mathrm{g}} & q_{\mathrm{g}} \end{bmatrix}^{\intercal}$, then it can be expressed by:

$$\boldsymbol{x}_p = \begin{bmatrix} v_{\mathrm{g}\alpha} & v_{\mathrm{g}\beta} \\ v_{\mathrm{g}\beta} & -v_{\mathrm{g}\alpha} \end{bmatrix} \boldsymbol{i}_{\mathrm{g}} = \mathbf{V}_{\mathrm{g}} \boldsymbol{i}_{\mathrm{g}} \tag{3.38}$$

To obtain a dynamic model for $\boldsymbol{x}_p$, the time derivative of (3.38) is taken as

$$\frac{\mathrm{d}\boldsymbol{x}_p}{\mathrm{d}t} = \frac{\mathrm{d}\mathbf{V}_{\mathrm{g}}}{\mathrm{d}t} \boldsymbol{i}_{\mathrm{g}} + \mathbf{V}_{\mathrm{g}} \frac{\mathrm{d}\boldsymbol{i}_{\mathrm{g}}}{\mathrm{d}t}. \tag{3.39}$$

Under a balanced sinusoidal three-phase grid system with an angular frequency ω_{g}, the time derivative of the grid voltage vector can be determined as [47] [83]:

$$\frac{\mathrm{d}\boldsymbol{v}_{\mathrm{g}}}{\mathrm{d}t} = \omega_{\mathrm{g}} \mathbf{J} \boldsymbol{v}_{\mathrm{g}} \quad ; \quad \mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}. \tag{3.40}$$

which implies that

$$\frac{\mathrm{d}\mathbf{V}_{\mathrm{g}}}{\mathrm{d}t} = \omega_{\mathrm{g}} \mathbf{J} \mathbf{V}_{\mathrm{g}}. \tag{3.41}$$

Therefore, by replacing (3.4) and (3.41) into (3.39), the following continuous-time state-space model for the apparent power vector can be expressed in terms of the switching vectors $\boldsymbol{u}_s$ as:

$$\dot{\boldsymbol{x}}_p = \boldsymbol{A} \boldsymbol{x}_p + \boldsymbol{B}(t) \boldsymbol{u}_s + \boldsymbol{\eta}(t) \tag{3.42}$$

with

$$\boldsymbol{A} = \begin{bmatrix} -R/L & -\omega_{\mathrm{g}} \\ \omega_{\mathrm{g}} & -R/L \end{bmatrix}, \tag{3.43}$$

and both, the known disturbance $\boldsymbol{\eta}(t)$ and the input matrix $\boldsymbol{B}(t)$ depending on the grid voltage vector as

$$\boldsymbol{\eta}(t) = -\frac{1}{L} \mathbf{V}_{\mathrm{g}}(t) \boldsymbol{v}_{\mathrm{g}}(t) \ , \quad \boldsymbol{B}(t) = \frac{V_{\mathrm{dc}}}{2L} \mathbf{V}_{\mathrm{g}}(t) \tag{3.44}$$

It is worth highlight here that (3.42) represents a second-order linear time-variant (LTV) system. However, by explicitly considering the 7S-SS in the formulation of the C-OSS-MPC strategy, the corresponding discrete-time model will take a more friendly structure for control purposes.

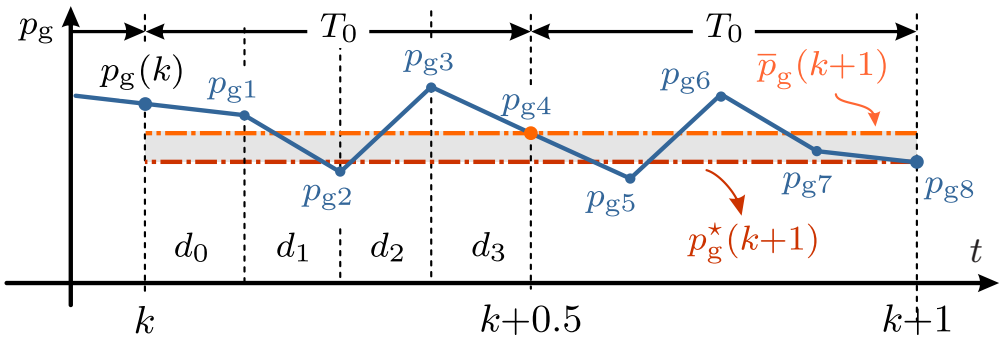

FIGURE 3.7: Predicted system trajectory for a 7S-SS.

3.7.2 Discrete-Time Model: The Average Trajectory

Following the same procedure introduced in section 3.3.2 for the OSS current control, the instantaneous evolution of the apparent power when a given 7S-SS as per (A.1) is synthesized by the 3L-NPC converter can be approximated by employing the one-step Euler method as

$$\boldsymbol{x}_{p(i+1)} = \boldsymbol{x}_{p(i)} + \left.\frac{\mathrm{d}\boldsymbol{x}_p}{\mathrm{d}t}\right|_i T_0 d_i \tag{3.45}$$

Because of the symmetrical nature of the 7S-SS, the average trajectory during a switching period is equal to the instantaneous value of $\boldsymbol{x}_p$ at the end of the sub-cycle, i.e., $\overline{\boldsymbol{x}}_p = \boldsymbol{x}_{p4}$, as illustrated in Fig. 3.7 for the active power only. Thus it can be expressed as

$$\overline{\boldsymbol{x}}_p(k{+}1) = \boldsymbol{x}_p(k) + T_0 \sum_{i=0}^{3} \left.\frac{\mathrm{d}\boldsymbol{x}_p}{\mathrm{d}t}\right|_i d_i \tag{3.46}$$

where the ith subinterval slope can be approximated by

$$\left.\frac{\mathrm{d}\boldsymbol{x}_p}{\mathrm{d}t}\right|_i = \boldsymbol{A}\boldsymbol{x}_p(k) + \boldsymbol{B}(k)\boldsymbol{u}_{si} + \boldsymbol{\eta}(k), \tag{3.47}$$

Hence, the the average trajectory (3.46) can be approximated by

$$\overline{\boldsymbol{x}}_p(k{+}1) = \boldsymbol{A}_0\boldsymbol{x}_p(k) + \boldsymbol{\eta}_0(k) + \boldsymbol{B}_0(k) \sum_{i=0}^{3} \boldsymbol{u}_{si} d_i \tag{3.48}$$

with $\boldsymbol{A}_0{=}\boldsymbol{I}{+}\boldsymbol{A}T_0$, $\boldsymbol{B}_0{=}T_0\boldsymbol{B}$ and, $\boldsymbol{\eta}_0{=}T_0\boldsymbol{\eta}$. Additionally, because of $\boldsymbol{u}_{\mathrm{S}}^{+} = \boldsymbol{u}_{\mathrm{S}}^{-}$, the following linear representation of the average trajectory can be stated:

$$\overline{\boldsymbol{x}}_p(k{+}1) = \boldsymbol{A}_0\boldsymbol{x}_p(k) + \boldsymbol{p}_0(k) + \boldsymbol{B}_0(k)\boldsymbol{U}(k)\boldsymbol{d}(k) \tag{3.49}$$

where, just like in the section 3.3.2, the duty cycle vector and the matrix switching vectors are

respectively defined as follows

$$\boldsymbol{d}(k) \triangleq \begin{bmatrix} d_{\mathrm{S}}(k) & d_2(k) & d_3(k) \end{bmatrix}^{\intercal} \in \mathbb{D} \triangleq [0,1]^3, \tag{3.50}$$

$$\boldsymbol{U}(k) \triangleq \begin{bmatrix} \boldsymbol{u}_{\mathrm{S}}(k) & \boldsymbol{u}_2(k) & \boldsymbol{u}_3(k) \end{bmatrix}, \tag{3.51}$$

with $d_{\mathrm{S}}{=}d_0{+}d_3$.

3.7.3 Optimal Control Problem for OSS-MP-DPC.

To obtain the optimal application times, the following quadratic cost function is introduced

$$J_p = \boldsymbol{e}_p^{\intercal}(k{+}1)\boldsymbol{e}_p(k{+}1) + \lambda_{\mathrm{u}}\Delta\boldsymbol{u}^{\intercal}(k)\Delta\boldsymbol{u}(k) \tag{3.52}$$

which is a suitable choice to penalize the predicted tracking error and the control input effort, where

$$\boldsymbol{e}_p(k{+}1) \triangleq \boldsymbol{x}_p(k{+}1){-}\boldsymbol{x}_p^*(k{+}1) \tag{3.53}$$

$$\Delta\boldsymbol{u}(k) \triangleq \boldsymbol{u}(k) - \boldsymbol{u}_{\mathrm{ss}}(k) \tag{3.54}$$

with $\boldsymbol{u}(k) = \boldsymbol{U}(k)\boldsymbol{d}(k)$ being the average switching vector applied by the converter and $\boldsymbol{u}_{\mathrm{ss}}(k)$ the required input to maintain the apparent power vector at the desired steady-state operating conditions [29]. Under this perspective, by using (3.42) with $\dot{\boldsymbol{x}}_p = 0$ and $\boldsymbol{x}_p(k) = \boldsymbol{x}_p^*$, the later can be expressed as:

$$\boldsymbol{u}_{\mathrm{ss}}(k) = -\boldsymbol{B}(k)^{-1}(\boldsymbol{A}\boldsymbol{x}_p^* + \boldsymbol{\eta}(k)) \tag{3.55}$$

Moreover, from (3.53), it follows that

$$\begin{aligned} \boldsymbol{e}_p(k{+}1) &= \boldsymbol{A}_0\boldsymbol{x}_p(k) + \boldsymbol{\eta}_0(k) + \boldsymbol{B}_0\boldsymbol{U}_j(k)\boldsymbol{d}_j(k) - \boldsymbol{x}_p^* \\ &= \boldsymbol{B}_0[\boldsymbol{U}_j(k)\boldsymbol{d}_j(k) - \underbrace{\boldsymbol{B}_0^{-1}(\boldsymbol{x}_p^* - \boldsymbol{A}_0\boldsymbol{x}_p(k) - \boldsymbol{\eta}_0(k))}_{\boldsymbol{u}_{\mathrm{db}}(k)}] \end{aligned} \tag{3.56}$$

with $\boldsymbol{u}_{\mathrm{db}}(k)$ being the deadbeat control input. It is worth to highlight that, unless a short-circuit at the point of common coupling (PCC) occurs, the matrix $\boldsymbol{B}_0$ is always invertible since

$$\boldsymbol{B}_0^{-1} = \frac{2L}{T_0 V_{\mathrm{dc}}} \frac{1}{V_{\mathrm{g}}^2(k)} \begin{bmatrix} v_{\mathrm{g}\alpha}(k) & v_{\mathrm{g}\beta}(k) \\ v_{\mathrm{g}\beta}(k) & -v_{\mathrm{g}\alpha}(k) \end{bmatrix} \tag{3.57}$$

where

$$V_{\mathrm{g}}^2(k) = v_{\mathrm{g}\alpha}^2(k) + v_{\mathrm{g}\beta}^2(k) \tag{3.58}$$

is the square of the grid voltage vector amplitude.

For the sake of space, the discrete-time index k will be omitted from now on. It follows that the

cost function (3.13) can be expressed as:

$$J_p = \big(\boldsymbol{U}\boldsymbol{d} - \boldsymbol{u}_{\mathrm{db}}\big)^{\intercal}\boldsymbol{B}_0^{\intercal}\boldsymbol{B}_0\big(\boldsymbol{U}\boldsymbol{d} - \boldsymbol{u}_{\mathrm{db}}\big) + \lambda_{\mathrm{u}}\big(\boldsymbol{U}\boldsymbol{d} - \boldsymbol{u}_{\mathrm{ss}}\big)^{\intercal}\big(\boldsymbol{U}\boldsymbol{d} - \boldsymbol{u}_{\mathrm{ss}}\big) \tag{3.59}$$

It is straightforward to show that in (3.59), the matrix $\boldsymbol{B}_0^{\intercal}\boldsymbol{B}_0$ is given by:

$$\boldsymbol{B}_0^{\intercal}\boldsymbol{B}_0 = \frac{V_{\mathrm{dc}}^2 T_0^2}{4L^2} V_{\mathrm{g}}^2(k)\mathbf{I}_2 \tag{3.60}$$

Therefore, the cost function can be finally expressed as:

$$J_p(\boldsymbol{d}, \boldsymbol{U}) = \lambda_{\mathrm{p}}\big\|\boldsymbol{U}\boldsymbol{d} - \boldsymbol{u}_{\mathrm{db}}\big\|_2^2 + \lambda_{\mathrm{u}}\big\|\boldsymbol{U}\boldsymbol{d} - \boldsymbol{u}_{\mathrm{ss}}\big\|_2^2 \tag{3.61}$$

where

$$\lambda_{\mathrm{p}} = \frac{V_{\mathrm{dc}}^2 T_0^2}{4L^2} V_{\mathrm{g}}^2(k) \tag{3.62}$$

Accordingly, when the ratio $\lambda_{\mathrm{u}}/\lambda_{\mathrm{p}}$ is too small, then the first term in (3.61) becomes predominant; and hence, the controller will have a structure similar to a multi-variable deadbeat controller. Conversely, if $\lambda_{\mathrm{u}}/\lambda_{\mathrm{p}}$ is too large, the optimal solution tends to $\boldsymbol{u}_{\mathrm{ss}}$ which result in open-loop operation. Therefore, the tuning parameter λ_{u} allows manipulating the closed-loop dynamic response.

As described in (3.61), the cost function has been expressed as a function of the normalized application times $\boldsymbol{d}$ and the matrix $\boldsymbol{U}$. Consequently, the OSS is obtained by solving, at each sampling instant k, the following OSS-DPC problem:

$$\{\boldsymbol{U}^{\star}, \boldsymbol{d}^{\star}\} = \arg\min_{\boldsymbol{U}_j}\Big\{\min_{\boldsymbol{d}_j}\ J_p(\boldsymbol{d}_j, \boldsymbol{U}_j)\Big\} \tag{3.63a}$$

$$\text{s.t.}\ \ \mathbb{1}^{\intercal}\boldsymbol{d}_j = 1 \tag{3.63b}$$

$$\boldsymbol{d}_j \geq 0. \tag{3.63c}$$

It is important to highlight that the COP for OSS-DPC in (3.63) has exactly the same structure that the one shown in (3.19) for OSS-CC. Furthermore, the cost function and constraints of the internal optimization stage shown in (3.63) define the same BCLS shown (3.19). Therefore, the same optimization algorithm for the Outer-MPC introduced in section 3.4 can be directly applied for solving the COP for OSS-DPC shown in (3.63).

It is worth to bear on mind that the only difference between the cost functions involved for both control purposes (please compare (3.16) for current control and (3.61) for direct power control), is the parameter λ_{i} and λ_{p}.

3.8 Implementation Issues

This section introduces some critical issues regarding the practically implementation of the proposed Cascaded-OSS-MPC strategies analysed earlier. In particular, the Pulse-Width-Modulation that was programmed in order to generate the OSS obtained from the proposed Cascaded-OSS-MPC strategies. Furthermore, a reduced order observer to obtain the grid-voltage vector with a proper rejection of the distortion in the utility waveform is also introduced in this section.

3.8.1 Grid-Voltage Observer (GVO)

As mentioned earlier, the presented predictive strategies for grid-connected 3L-NPC converters depend on the accuracy with which the grid-voltage vector $\boldsymbol{v}_{\mathrm{g}}$ is computed within the control algorithm. Both in the current control and the active/reactive power control, the unconstrained solution depends on the estimated grid-voltage vector.

To be more specific, the matrices $\boldsymbol{B}(k)$ and $\boldsymbol{\eta}(k)$ depend on the grid-voltage at the point of common coupling (PCC). Therefore, they are susceptible to the distortion in the utility voltage waveform due to the high-frequency grid-current ripple (voltage drop across the inductor) [10], especially when a large short-circuit inductance is between the ideal voltage source and the PCC, as in the case of the experimental setup shown in Fig. 4.8. This ripple is concentrated at the equivalent switching frequency of the converter, which is twice the switching period f_{s} [76].

To overcome this problem, a closed-loop observer is adopted in this investigation effort to remove the grid voltage ripple by using the β-component of the grid voltage vector as the only measured input. Thus, the observer is based on the discrete-time version of (3.40) as follows:

$$\hat{\boldsymbol{v}}_{\mathrm{g}}(k{+}1) = \boldsymbol{\Phi}\,\hat{\boldsymbol{v}}_{\mathrm{g}}(k) - \boldsymbol{L}\boldsymbol{C}\big(\boldsymbol{v}_{\mathrm{g}}(k) - \hat{\boldsymbol{v}}_{\mathrm{g}}(k)\big) \tag{3.64}$$

with

$$\boldsymbol{\Phi} = \begin{bmatrix} \cos(T_{\mathrm{s}}\omega_{\mathrm{g}}) & -\sin(T_{\mathrm{s}}\omega_{\mathrm{g}}) \\ \sin(T_{\mathrm{s}}\omega_{\mathrm{g}}) & \cos(T_{\mathrm{s}}\omega_{\mathrm{g}}) \end{bmatrix} \tag{3.65}$$

and

$$\boldsymbol{C} = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{3.66}$$

In (3.64), the gain matrix $\boldsymbol{L} = \begin{bmatrix} \ell_1 & \ell_2 \end{bmatrix}^{\intercal}$ allows one to place the closed-loop poles at desired locations. Thereby, the observer closed-loop characteristic equation in the z-domain is given by

$$\det\big(z\boldsymbol{I} - (\boldsymbol{\Phi} + \boldsymbol{L}\boldsymbol{C})\big) = z^2 + p_1 z + p_2. \tag{3.67}$$

Thus, the coefficients p_1 and p_2 can be expressed as function of the desired damping ζ and natural

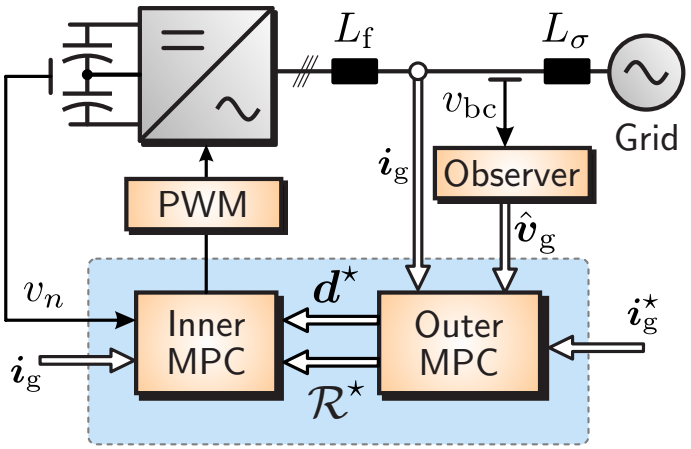

FIGURE 3.8: Proposed C-OSS-MPC for current control.

frequency $\omega_\mathrm{n} = 2\pi f_\mathrm{n}$ as [84]:

$$\begin{aligned} p_1 &= -2\mathrm{e}^{-\zeta\omega_\mathrm{n}T_\mathrm{s}}\cos\left(\omega_\mathrm{n}T_\mathrm{s}\sqrt{1-\zeta^2}\right) \\ p_2 &= \mathrm{e}^{-2\zeta\omega_\mathrm{n}T_\mathrm{s}}. \end{aligned} \tag{3.68}$$

Hence, by solving (3.67), the components of $\boldsymbol{L}$ are given by

$$\begin{aligned} \ell_1 &= \frac{p_1\cos(T_\mathrm{s}\omega_\mathrm{g}) + 2\cos^2(T_\mathrm{s}\omega_\mathrm{g}) + p_2 - 1}{\sin(T_\mathrm{s}\omega_\mathrm{g})} \\ \ell_2 &= p_1 + 2\cos(T_\mathrm{s}\omega_\mathrm{g}). \end{aligned} \tag{3.69}$$

Besides, because $v_{\mathrm{g}\beta} = v_\mathrm{bc}/\sqrt{3}$, with v_bc the measured line c-to-b voltage, the closed-loop observer is finally expressed as:

$$\begin{bmatrix} \hat{v}_{\mathrm{g}\alpha}(k+1) \\ \hat{v}_{\mathrm{g}\beta}(k+1) \end{bmatrix} = \begin{bmatrix} \cos(T_\mathrm{s}\omega_\mathrm{g}) & -\sin(T_\mathrm{s}\omega_\mathrm{g}) \\ \sin(T_\mathrm{s}\omega_\mathrm{g}) & \cos(T_\mathrm{s}\omega_\mathrm{g}) \end{bmatrix} \begin{bmatrix} \hat{v}_{\mathrm{g}\alpha}(k) \\ \hat{v}_{\mathrm{g}\beta}(k) \end{bmatrix} - \begin{bmatrix} \ell_1 \\ \ell_2 \end{bmatrix} \left(\frac{v_\mathrm{bc}(k)}{\sqrt{3}} - \hat{v}_{\mathrm{g}\beta}(k) \right) \tag{3.70}$$

where the components of $\boldsymbol{L}$ are computed to achieve the desired natural frequency of $f_\mathrm{n} = 30$ Hz with damping $\zeta = 0.8$. The resulting parameters ℓ_1 and ℓ_2 are shown in Table 4.2. Fig. 3.8 shows the bolck diagram of the proposed C-OSS-MPC for current control considering the grid-voltage observer given in (3.70).

It is worth noting that (3.64) is, indeed, a predictor-observer. Therefore, the observed grid-voltage vector $\hat{\boldsymbol{v}}_\mathrm{g}(k+1)$ can be directly used to compensate the inherent one sampling period delay of digital platforms. Additional discussion and analysis concerning this topic will be addressed in section 4.6.2.

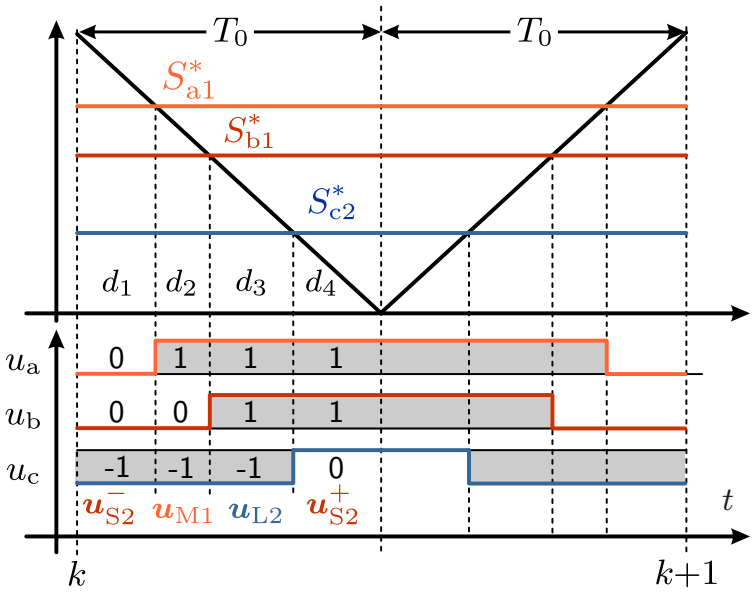

FIGURE 3.9: Single-carrier-based PWM for 3L-NPC converters.

3.8.2 Single-Carrier-Based PWM

As illustrated in Fig. 3.8, a single-carrier-based modulation technique is proposed in this work to produce the OSS that is obtained from the C-OSS-MPC strategy. The main challenge of the modulation stage is to determine the signal reference for each semiconductor device, S^*_{x1}, $S^*_{x2} \in [0, 1]$, in terms of the switching vectors $\boldsymbol{u}_{si}$ and their corresponding normalized application times d_i that generate the desired OSS.

As depicted in the circuit diagram of Fig. 3.1, each converter leg $x \in \mathcal{P}=\{a, b, c\}$ is controlled by two gate signals, s_{x1} and $s_{x2} \in \{0, 1\}$. Hence, according to the feasible switching state of the 3L-NPC converter shown in Table 2.1, the inverter switching states can be expressed in terms of these gate signals as

$$u_x = s_{x1} + s_{x2} - 1 \tag{3.71}$$

Based on the basis of PWM, an average model of the converter is derived in the following. In this regard, we first denote

$$U_x = \frac{1}{T_s} \int_0^{T_s} u_x(t) \mathrm{d}t \in [-1, 1] \tag{3.72}$$

as the duty cycle for x-leg of the inverter. Under this perspective (3.71) leads to

$$U_x = S_{x1} + S_{x2} - 1, \tag{3.73}$$

in which S_{x1} and $S_{x2} \in [0, 1]$ are the device duty-cycles.

As was previously discussed, each 7S-SS is built to get just one commutation per phase during

a switching cycle and direct transitions between the states $+1$ and -1 are not allowed. Thereby, during the whole switching period, each converter leg is switching either between 0 and $+1$ or between 0 and -1. Therefore, the reference signal to be modulated in the x-leg of the converter can be expressed as

$$U_{\mathrm{x}}^{\star} = \sum_{i=1}^{4} d_i \, u_{\mathrm{x}}(\boldsymbol{u}_{si}) \in [-1, 1] \quad \mathrm{x} \in \mathcal{P}{=}\{\mathrm{a}, \mathrm{b}, \mathrm{c}\} \tag{3.74}$$

where $u_x(\boldsymbol{u}_i){\in}\{-1, 0, 1\}$, is the x-leg switching state associated to the ith switching vector that belongs to the OSS.

According to the feasible switching states of the 3L-NPC converter shown in Table 2.1, if $U_{\mathrm{x}}^{*} \geq 0$, the gate signal reference (signal to be compared with the carrier signal u_{tr}) associated with the second semiconductor is necessary $U_{\mathrm{x2}}^{*} = 1$. Hence, to satisfy (3.73), the reference signal U_{x}^{*} has to directly be assigned to the first gate signal as $U_{\mathrm{x1}}^{*} = U_{\mathrm{x}}^{*}$. Conversely, if the reference signal computed using (3.74) is negative, i.e., $U_{\mathrm{x}}^{*} < 0$, thus $U_{\mathrm{x1}}^{*} = 0$ and $U_{\mathrm{x2}}^{*} = U_{\mathrm{x}}^{*} + 1$.

Fig. 3.9 shows an illustrative example for the modulation technique proposed in this work. According to (3.74), the reference signals that allow producing the 7S-SS shown in Fig. 3.9 are given by

$$U_{\mathrm{x}}^{*} = d_1 u_{\mathrm{x}}(\boldsymbol{u}_{\mathrm{S2}}^{-}) + d_2 u_{\mathrm{x}}(\boldsymbol{u}_{\mathrm{M1}}) + d_3 u_{\mathrm{x}}(\boldsymbol{u}_{\mathrm{L2}}) + d_4 u_{\mathrm{x}}(\boldsymbol{u}_{\mathrm{S2}}^{+})$$

Therefore, the reference signals associated to each semiconductor are expressed in terms of the dwell times as

$$\begin{aligned} U_{\mathrm{a1}}^{*} = d_2 + d_3 + d_4 \quad &\wedge \quad U_{\mathrm{a2}}^{*} = 1 \\ U_{\mathrm{b1}}^{*} = d_3 + d_4 \quad &\wedge \quad U_{\mathrm{b2}}^{*} = 1 \\ U_{\mathrm{c1}}^{*} = 0 \quad &\wedge \quad U_{\mathrm{c2}}^{*} = 1 - d_1 - d_2 - d_3 \end{aligned}$$

Notice that using the proposed single-carrier-based PWM scheme, the switching vectors and their application times are directly mapped to the commutation devices duty cycles in order to synthesize the required OSS.

3.8.3 Summary

This Chapter has presented the proposed Cascaded OSS-MPC strategy for both grid-current control and direct active/reactive power control of grid-connected 3L-NPC converts. This proposal considers a cascade structure as depicted in Fig. 3.8.

On one hand, the first stage (Outer-MPC) controls the average trajectory of the output current or active/reactive power with a robust and computationally efficient OSS-MPC strategy. This external MPC controller provides a set of switching vectors and their optimal applications times during either steady-state and transients operating conditions.

On the other hand, the second stage (Inner-MPC) is utilised to balancing the capacitor voltages of the converter by using an explicit optimal control law to handle the redundancy of the 3L-NPC converter, avoiding the use of weighting factors.

Furthermore, an efficient optimization algorithm is addressed in this Chapter to reduce the computational burden typically observed in the OSS-MPC strategies. This algorithm promptly finds the optimal solution in order to make possible a real-time implementation of the proposed control strategy in standard digital control platforms.

Finally, implementation issues are discussed concerning the carrier-based PWM stage to produce the desired OSS. Besides, a reduced-order observer is also introduced to reject the distortion in the utility voltage waveforms and to improve the performance of the controlled system.

CHAPTER 4

Simulation and Experimental Results

In this Chapter, the simulations and experimental results to validate and evaluate the performance of the proposed MPC strategies for grid-connected 3L-NPC converters are introduced in detail for both current control and active/reactive power control.

The 3L-NPC converter has been operated feeding a passive load to obtain performance indexes such THD and average tracking error over the whole range of modulation index. Besides, in the grid-connected mode, the experimental validation has been made for several power factors and transient operating conditions. The performance and effectiveness of the Inner-MPC stage focusing on the capacitor voltage balancing is also evaluated and validated experimentally.

The proposed cascaded OSS-MPC was implemented in a standard DSP, which means that the final computational burden to obtain the optimal solution has been kept low. The sensitivity analysis is also presented in this chapter, which allows understanding the effect of an error in the inductance value over the performance of the controlled system.

TABLE 4.1: Simulations Parameters.

Name	Param.	Value	Name	Param.	Value
Resistance Filter	R	0.1 Ω	DC-voltage	$V_{\rm dc}$	600 V
Inductance Filter	L	2.5 mH	Grid voltage	$V_{\rm g}$	$\sqrt{2/3}\cdot 380$ V
Capacitance	C_1=C_2	300 μF		$\lambda_{\rm i}=\frac{V_{\rm dc}^2 T_0^2}{4L^2}$	576 A^2
Sampling period	$T_{\rm s}$	400 μs	Tuning	$\lambda_{\rm u}=\lambda_{\rm i}$	576

4.1 Performance Indexes

To measure the performance of the proposed controller, the following indexes are considered: the well-known total harmonic distortion (THD) and the weighted THD (WTHD) of the output current and the inverter line-to-line voltages, and the average current tracking error. In this work, the latter is defined as

$$E_I[\%]=\frac{100}{\|\boldsymbol{i}_{\rm g}^{\star}\|}\sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{N}}\left\|\overline{\boldsymbol{i}_{\rm g}}(k)-\boldsymbol{i}_{\rm g}^{\star}(k)\right\|_2^2} \tag{4.1}$$

where N_p=T_1/T_s is the number of samples per fundamental cycle, and the set $\mathcal{N}$=$\{1,\ldots,\,N_p\}$.

On the other hand, the modulation index m is defined as the ratio between the magnitude of the optimal average switching vector (OASV) and the radius of the largest inscribed circle within the hexagon shown in Fig. 2.7. Hence, it is computed as

$$m=\frac{\sqrt{3}}{2}\frac{1}{N_p}\sum_{k\in\mathcal{N}}\sqrt{u_{{\rm s}\alpha}^{\star}(k)^2+u_{{\rm s}\beta}^{\star}(k)^2} \tag{4.2}$$

where the OASV is given by $\boldsymbol{u}_{\rm s}^{\star}(k)=\left[u_{{\rm s}\alpha}^{\star}(k)\;u_{{\rm s}\alpha}^{\star}(k)\right]^{\mathsf{T}}$

4.2 Simulation Results

In this section, the performance of the Cascaded-OSS-MP-CC strategy is evaluated by performing several simulations with the software *block set* of PLECS for MATLAB. The main target of the simulations is to validate the capability of the proposed optimizer shown in Fig. 3.6 to find the actual optimal solution of the constrained optimization problem defined in (3.19).

The parameters of the system are summarized in Table 4.1. It is worth to highlight that the tuning parameter of the controller is designed to have the same relevance for both objectives in the cost function, which means that $\lambda_{\rm u}=\lambda_{\rm i}$.

The simulation tests consist of operating the converter with desired active and reactive power $p_{\rm g}^{\star}(k)$ and $q_{\rm g}^{\star}(k)$, respectively. These instantaneous power references are indirectly controlled by

using the following grid current reference

$$\begin{bmatrix} i^{\star}_{g\alpha}(k+1) \\ i^{\star}_{g\beta}(k+1) \end{bmatrix} = \frac{2}{3V_g^2} \begin{bmatrix} v_{g\alpha}(k+1) & v_{g\beta}(k+1) \\ v_{g\beta}(k+1) & -v_{g\alpha}(k+1) \end{bmatrix} \begin{bmatrix} p^{\star}_{g}(k) \\ q^{\star}_{g}(k) \end{bmatrix} \tag{4.3}$$

where $V_g^2 = v_{g\alpha}^2 + v_{g\beta}^2$.

Fig. 4.1 shows the capacitor voltages and grid currents in the $\alpha\beta$ framework as well as the active and reactive power when several step changes in the active power reference $p_g^{\star}$ are applied considering unity power factor operation ($p_g^{\star}$=$\{0, 10, -10, 0\}$[kW]). The first one is applied at t≈65 [ms]. As shown in Fig. 4.1(a), a fast dynamic response with a minimum average active and reactive power tracking error is achieved with the proposed controller. Besides, the capacitor voltages are balanced even during the inversion of the power flow injected by the converter, as depicted in Fig. 4.1(b). It is important to highlight that the proposed Inner-MPC does not require additional information about the operating mode of the converter (motoring/generating) to balance the capacitor voltages efficiently. As depicted in Fig. 4.1(c) a good tracking of the current is achieved with the proposed Cascaded-OSS-MP-CC. Moreover, a fast dynamic response is also reached as it is concluded from the zoom of the grid currents depicted in Fig. 4.2.

Additionally, to validate the effectiveness and optimality of the proposed algorithm shown in

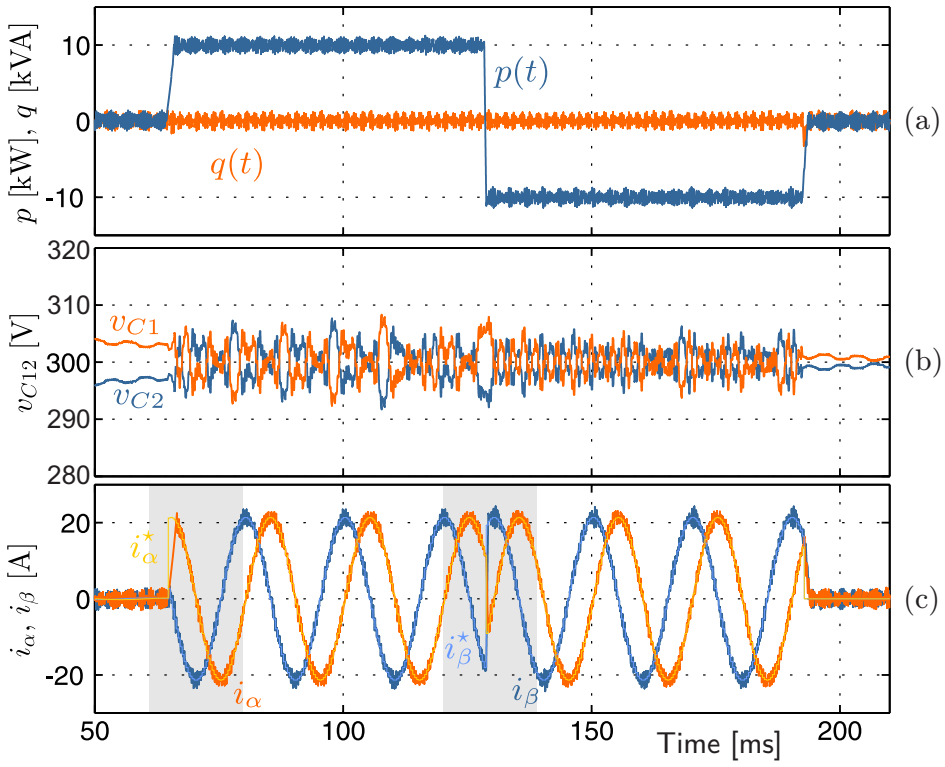

FIGURE 4.1: Simulation results for Cascaded-OSS-MP-CC: (a) active and reactive power; (b) capacitor voltages and; (c) grid currents.

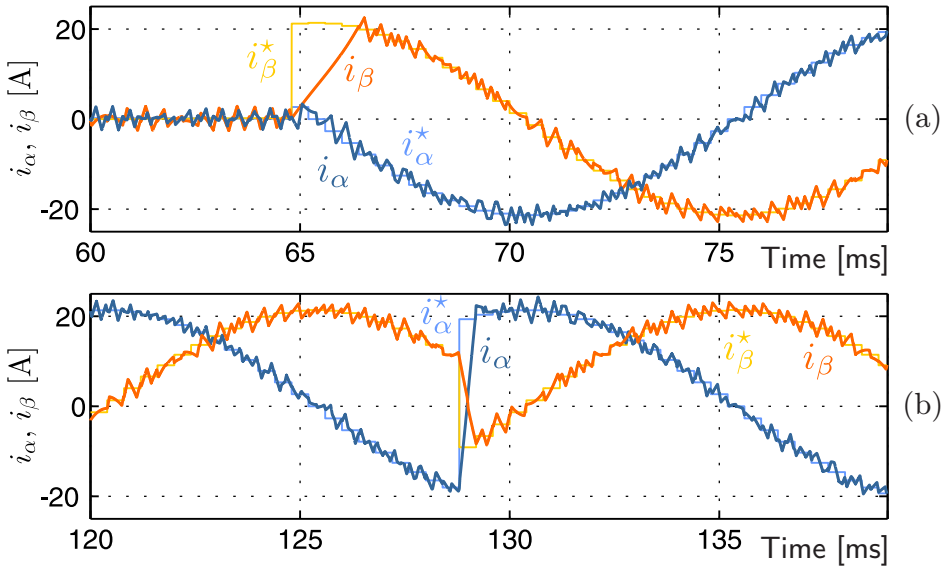

FIGURE 4.2: Zoom of the grid currents and their references for the first two step changes shown in Fig. 4.1: (a) first step-change and; (b) second step-change.

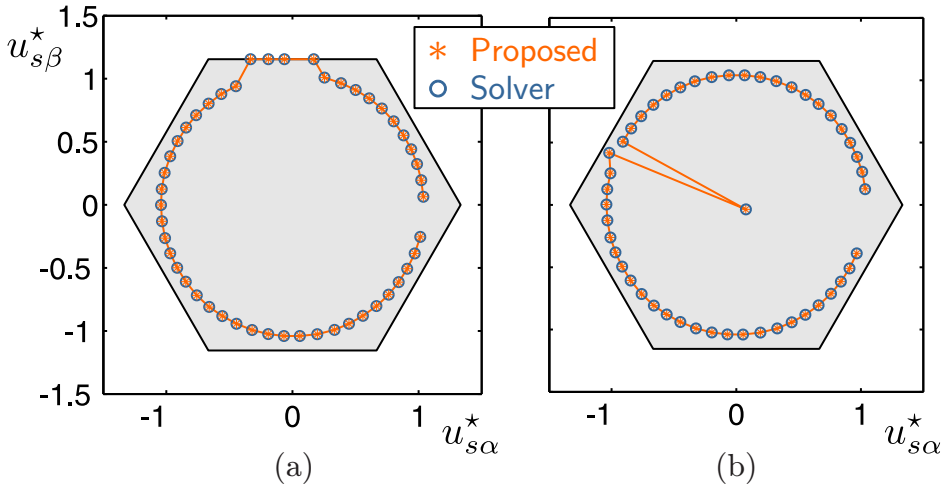

FIGURE 4.3: Comparison of the trajectories obtained (MATLAB' solver *LSQLIN* v/s proposed algorithm) for the optimal average switching vector $\boldsymbol{u}^\star_s = \left[u^\star_{s\alpha}\ \ u^\star_{s\beta}\right]^\mathsf{T}$.

Fig. 3.6, the trajectory of the optimal average switching vector $\boldsymbol{u}^\star_s(k)$ is compared with that obtained using an enumeration algorithm, where the internal optimization problem in (3.19) is solved for all $\mathcal{R} \in \boldsymbol{\mathcal{R}}$ using the MATLAB' solver *LSQLIN*. The comparison depicted in Figs. 4.3 shows that the proposed algorithm produces the same OASV than that achieved from the enumeration algorithm for the two power reference step-change variations depicted in Figs. 4.2. This fact demonstrates the capability of the proposed algorithm to compute the optimal switching sequence even during transient operating conditions of the power inverter.

Finally, Fig. 4.4 shows the steady-state harmonic spectra of the grid current operating with 10 kW and unity power factor. As shown in Fig. 4.4, a shaped harmonic spectrum is imposed by

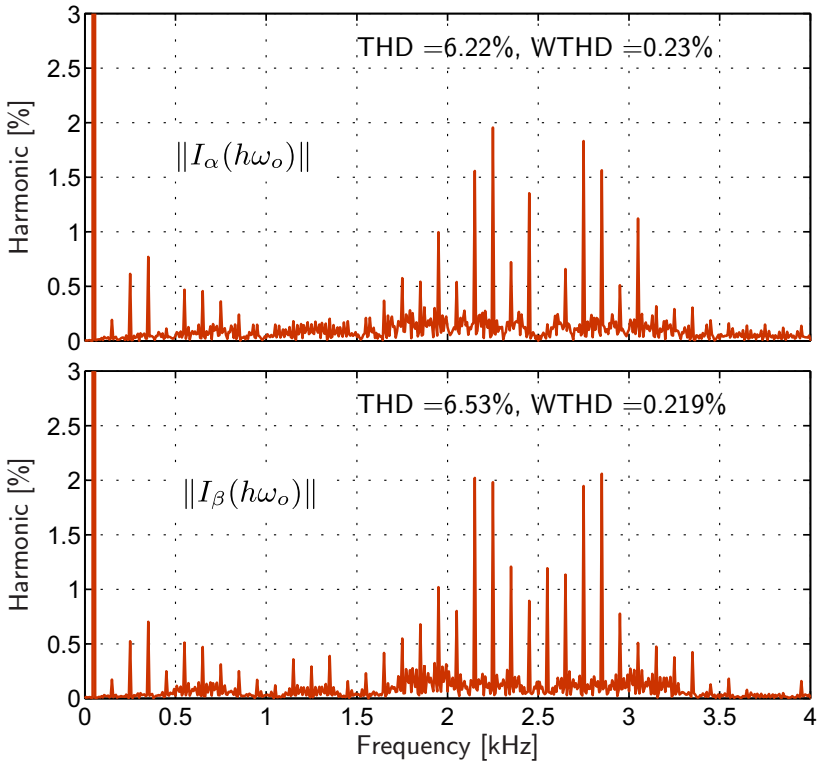

FIGURE 4.4: Harmonic spectrum of grid currents for $f_s = 2.5$ kHz.

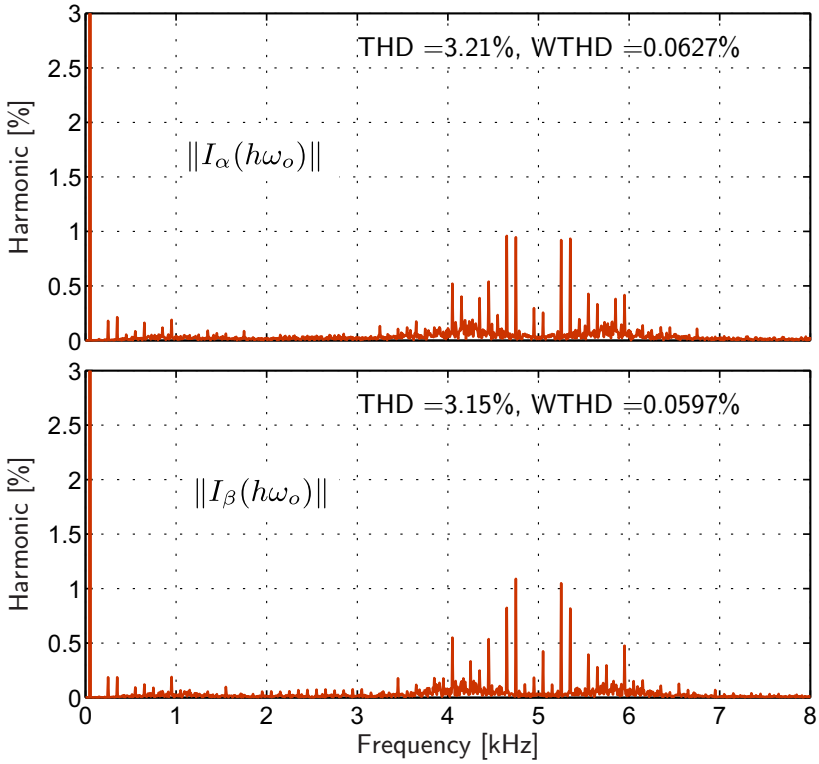

FIGURE 4.5: Harmonic spectrum of grid currents for $f_s = 5.0$ kHz

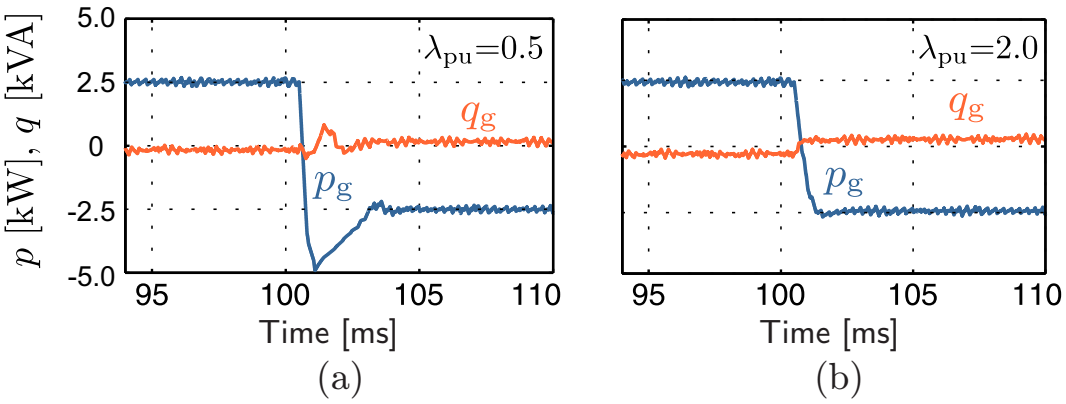

FIGURE 4.6: Effect of an overestimated inductance ($\mu_L = 1.5$) on the controlled system performance for two values of the weighting factor considering $f_s = 2$kHz and $V_{\rm dc} = 300$V: (a) $\lambda/\lambda_0 = 0.5$; and (b) $\lambda/\lambda_0 = 2.0$.

the control system where the amplitude amplitude of the harmonic components are below to 2% achieving a very good THD for the $\alpha\beta$ components of the three-phase currents. The high-frequency components are around the switching cycle frequency given by $f_{\rm s}$=2.5 kHz. Furthermore, as shown in Fig. 4.5, by implementing the switching sequence with twice the switching cycle frequency $f_{\rm s}$=5.0 kHz, the THD is almost reduced to the half maintaining the same shaping of the grid-current spectrum. The only difference is that the high-frequency harmonics are shifted around 5.0 kHz Therefore, the switching cycle frequency can be considered as another degree of freedom in order to fulfil the power quality requirements.

4.2.1 Sensitivity Analysis

To analyse the influence of model parametric uncertainties on the performance of the proposed predictive strategy, the parameter mismatches are modeled as $\hat{L} = \mu_L L_0$ and $\hat{R} = \mu_R R_0$ [85]. Under this perspective, it is straightforward to demonstrate that the deadbeat voltage error, defined as $\Delta \boldsymbol{v}_{\rm db} = 1/2V_{\rm dc}(\boldsymbol{u}_{\rm db} - \hat{\boldsymbol{u}}_{\rm db})$, can be expressed as:

$$\Delta \boldsymbol{v}_{\rm db} = \frac{L_0}{T_0}(1-\mu_L)\big(\boldsymbol{i}_{\rm g}^{\star}(k{+}1) - \boldsymbol{i}_{\rm g}(k)\big) + R_0(1-\mu_R)\,\boldsymbol{i}_{\rm g}(k) \tag{4.4}$$

As shown in (4.4), $\Delta \boldsymbol{v}_{\rm db}$ is not only determined by the parameters mismatch but also by the instantaneous values of the tracking error and the grid current vector. Thereby, $\Delta \boldsymbol{v}_{\rm db}$ is very susceptible to inductance mismatches during transient operation in which the tracking error $\boldsymbol{i}_{\rm g}^{\star}(k{+}1) - \boldsymbol{i}_{\rm g}(k)$ becomes predominant. Moreover, because the resistance is minimised during the design of a typical output filter, i.e., $L_0 \gg T_0 R_0$, the error in the resistance does not produce a significant effect on the deadbeat voltage error.

Fig. 4.6 shows the transient response for the worse case condition (where the reference current $\boldsymbol{i}_{\rm g}^{*}$ is suddenly shifted in 180) when an overestimated inductance value is used in the control algorithm.

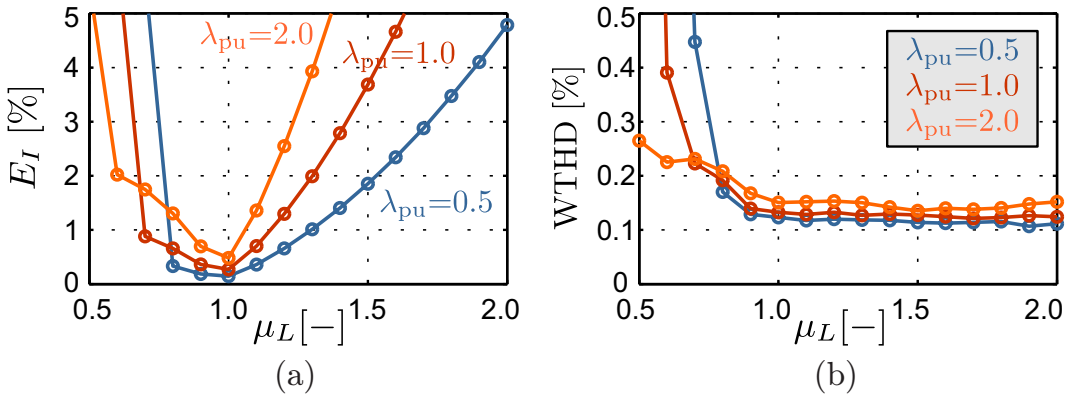

FIGURE 4.7: Effect of modelled value inductance errors on (a) average current tracking error E_I, and (b) WTHD considering $f_s = 2$kHz and $V_{\rm dc} = 300$V.

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As depicted in Fig. 4.6, the transient response is more susceptible to inductance estimation errors when the dead-beat control input becomes predominant because a low value for the weighting factor is utilised. This result confirms the conclusions which can be derived from (4.4). Using $\lambda_{\rm pu} = \lambda/\lambda_0 = 0.5$, the active power plummeted down to -5 kW, while for $\lambda_{\rm pu} = 1.5$, the undershoot is negligible. Therefore, for the proposed controller, the negative effect of L-variations over the closed-loop dynamic performance can be mitigated with a suitable design of the weighting factor.

In the same manner, using (3.15), the error in the steady-state voltage due to parameter uncertainties is given by

$$\Delta \boldsymbol{v}_{\rm ss} = \omega_{\rm g} L_0 (1-\mu_L) \mathbf{J} \boldsymbol{i}_{\rm g}^{\star}(k+1) + R_0 (1-\mu_R)\, \boldsymbol{i}_{\rm g}^{\star}(k+1) \tag{4.5}$$

According to the cost function, if $\lambda_{\rm u}$ is increased, the controlled system performance is more affected by $\Delta \boldsymbol{v}_{\rm ss}$ which depends on the instantaneous value of the grid current vector reference.

Fig. 4.7 shows the performance of the system in steady-state operating conditions considering a wide variation in the parameter μ_L. As depicted in Fig. 4.7(a), the average current tracking error E_I is reduced for lower values of $\lambda_{\rm pu}$. In this regard, it is recommended to avoid the zones where μ_L>1.3 or μ_L<0.8 to maintain the average tracking error below 1%. Moreover, for $\mu_L > 0.8$, the WTHD is lower than 0.2% and do not vary considerably for different values of $\lambda_{\rm pu}$.

In addition, the modified prediction model when the filter parameters are not well estimated can be obtained from (3.10) as:

$$\hat{\boldsymbol{i}}_{\rm g}(k{+}1) = \hat{\alpha}_1 \boldsymbol{i}_{\rm g}(k) + \hat{\alpha}_2 \boldsymbol{v}_{\rm g}(k) + \hat{\beta} \boldsymbol{U}(k) \boldsymbol{d}(k), \tag{4.6}$$

with $\hat{\alpha}_1{=}1{-}T_0 \frac{\mu_R R_0}{\mu_L L_0}$, $\hat{\alpha}_2{=}-\frac{T_0}{\mu_L L_0}$, $\hat{\beta}{=}\frac{1}{2} V_{\rm dc} \frac{T_0}{\mu_L L_0}$.

Thereby, the prediction error $\boldsymbol{e}_m(k{+}1) = \boldsymbol{i}_{\mathrm{g}}(k{+}1) - \hat{\boldsymbol{i}}_{\mathrm{g}}(k{+}1)$ can be expressed according to

$$\boldsymbol{e}_m = T_0 \frac{R_0}{L_0}\left(\frac{\mu_R}{\mu_L} - 1\right)\boldsymbol{i}_{\mathrm{g}}(k) + \frac{T_0}{L_0}\left(1 - \frac{1}{\mu_L}\right)(\boldsymbol{v}_{\mathrm{s}}(k) - \boldsymbol{v}_{\mathrm{g}}(k)). \tag{4.7}$$

As shown in (4.7), the prediction error depends on $\boldsymbol{i}_{\mathrm{g}}(k)$, which is measured at each sampling step of the predictive algorithm. It also depends on the converter and grid voltage vector. From (4.7), it is concluded that the prediction error is more susceptible when the inductance is underestimated, i.e., $\mu_L < 1$. For this reason, the simulations depicted in Fig. 4.7 were only carried out up to $\mu_L = 0.5$.

4.3 Experimental Results

The grid-connected 3L-NPC converter illustrated in Fig. 3.3 has been practically implemented to verify the theoretical and simulation work proposed in this theses. In this regard, this section presents experimental results for the Cascaded-OSS-MPC strategies introduced in Chapter 3.

4.3.1 Experimental Setup

The control algorithm shown in Fig. 3.6 was implemented in a DSP board based on the Texas Instrument DSK6713 platform augmented with a Xilinx FPGA Spartan 6 based board, as shown Fig. 4.8. Optical fiber links are used to transmit the switching signals to the IGBT gate drivers. The FPGA platform is programmed to handle the analogue to digital converters as well as to implement the modulator. More details regarding the experimental system and its implementation are shown in the Appendix

Experimental tests include steady-state and dynamic conditions for both passive RL-load and grid-connected configurations. The system parameters are summarized in Table 4.2.

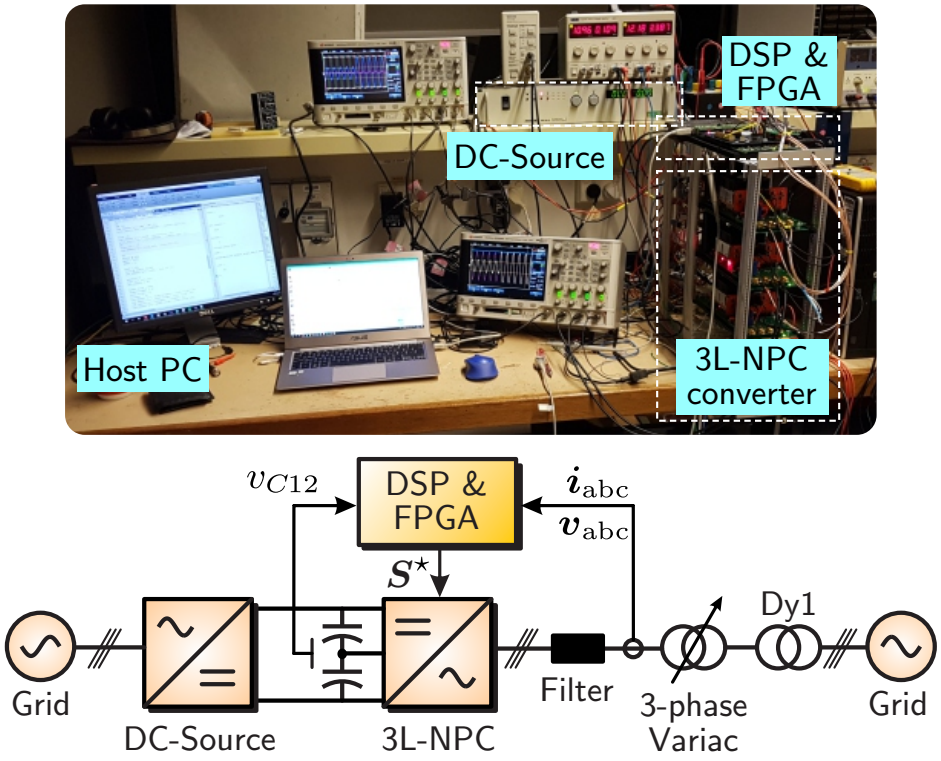


FIGURE 4.8: Experimental setup

TABLE 4.2: Main System and Controller Parameters.

Name	Param.	Value	Grid-voltage observer
Resistance Filter	R	0.35 Ω	$f_{\mathrm{n}} = 30$ Hz
Inductance Filter	L	3.9 mH	$\zeta = 0.8$
Capacitance	C_1=C_2	1800 μF	$\ell_1 = -8.207\times10^{-2}$
Sampling period	T_{s}	300 μs	$\ell_2 = 5.104\times10^{-2}$

4.4 Current Control of a Passive RL-Load

Firstly, to obtain the performance indexes over the whole range of modulation index, the experiments were carried out with the 3L-NPC converter feeding a passive RL-load whose parameters are $R = 10\,\Omega$ and $L_{\mathrm{f}} = 3.9$ mH. For this case, the same control algorithm shown in Fig. 3.6 and Fig. 3.8 is used by setting $\boldsymbol{v}_{\mathrm{g}}$=0.

The tracking error E_I and the THD of the line-to-line innverter voltages versus m are summarized in Fig. 4.9. From this figure, it is concluded that the THD along the whole modulation index range is very similar to that obtained from simulations realised in open-loop mode (just using SVM) without load [76]. On the other hand, focusing on the average tracking error, the proposed controller leads to an average error less than 1% for m>0.75 and considering two values of λ_{u}=$\{10, 100\}$. It is shown that the controller regulates very well the average trajectory of the output current, especially for higher modulation indexes, which corresponds to the normal operating conditions for grid-connected power converters.

The $\alpha\beta$ components of the output current and converter voltage waveforms for two particular modulation indexes m=$\{0.54,\ 0.89\}$ are shown in Fig. 4.10. The inverter phase voltage v_{an} is composed of three voltage levels, meanwhile the line-to-line voltage synthesised by the converter has five voltage levels when m≥0.5 is utilised. The differences between adjacent voltage levels are

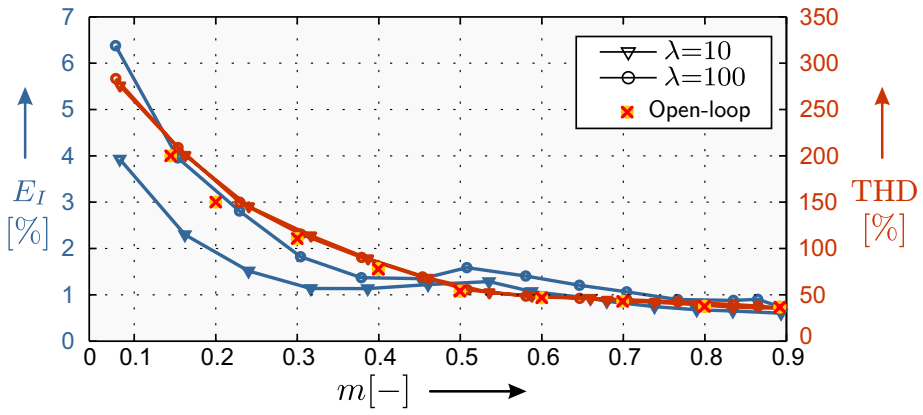


FIGURE 4.9: RL-Load: E_I (blue lines) and THD of the inverter line-to-line voltage (red lines) as a function of the modulation index for two values of the parameter λ_{u}=$\{10, 100\}$ at f_s=2kHz.

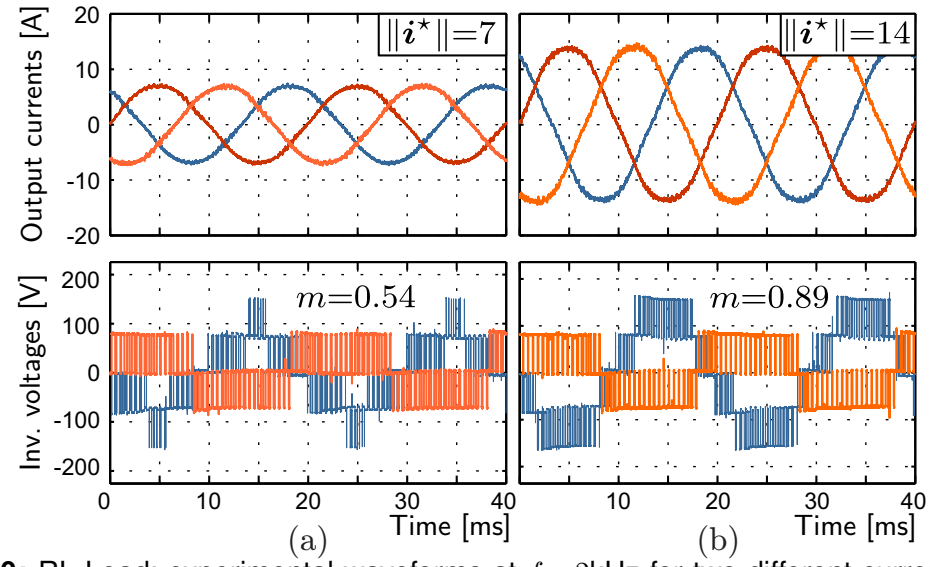


FIGURE 4.10: RL-Load: experimental waveforms at f_s=2kHz for two different current references $\|i^\star\|$ with $\lambda_u = 100$: (a) 7A (m=0.54) and; (b) 14A (m=0.89).

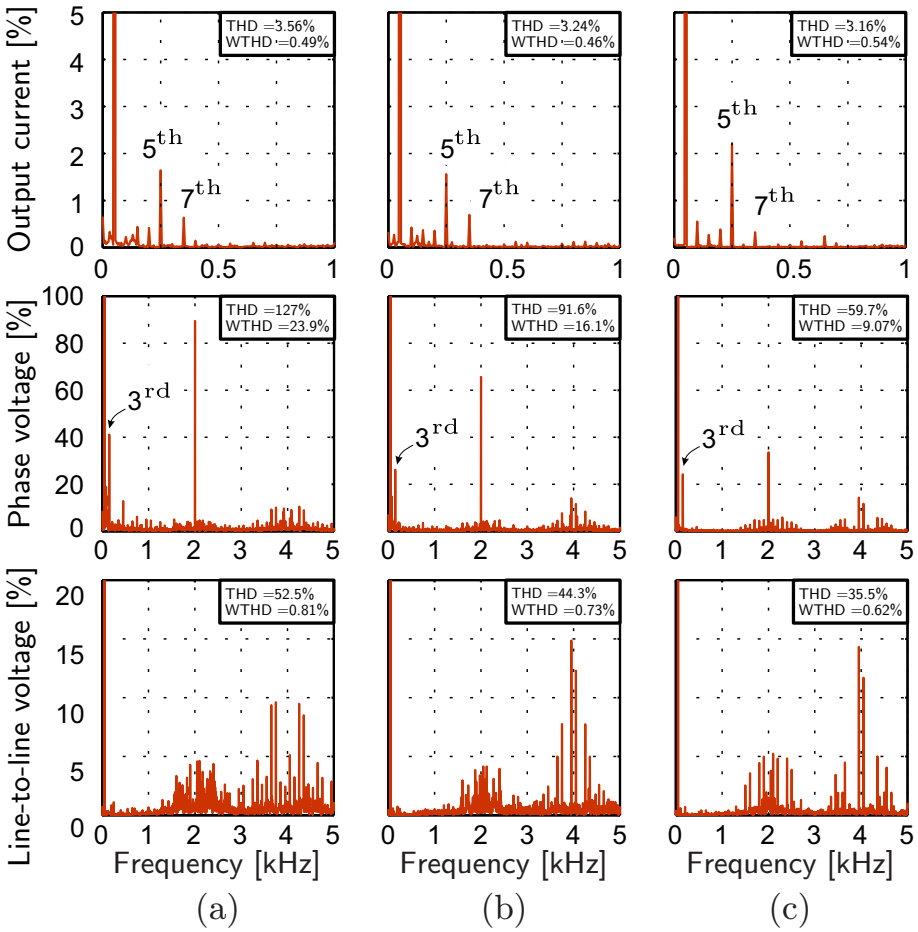


FIGURE 4.11: RL-Load: Harmonic Spectrum at f_s=2kHz for three different current references $\|i^\star\|$ with λ={10, 100}: (a) 7A (m=0.54); (b) 10A (m=0.68); (c) 14A (m=0.89).

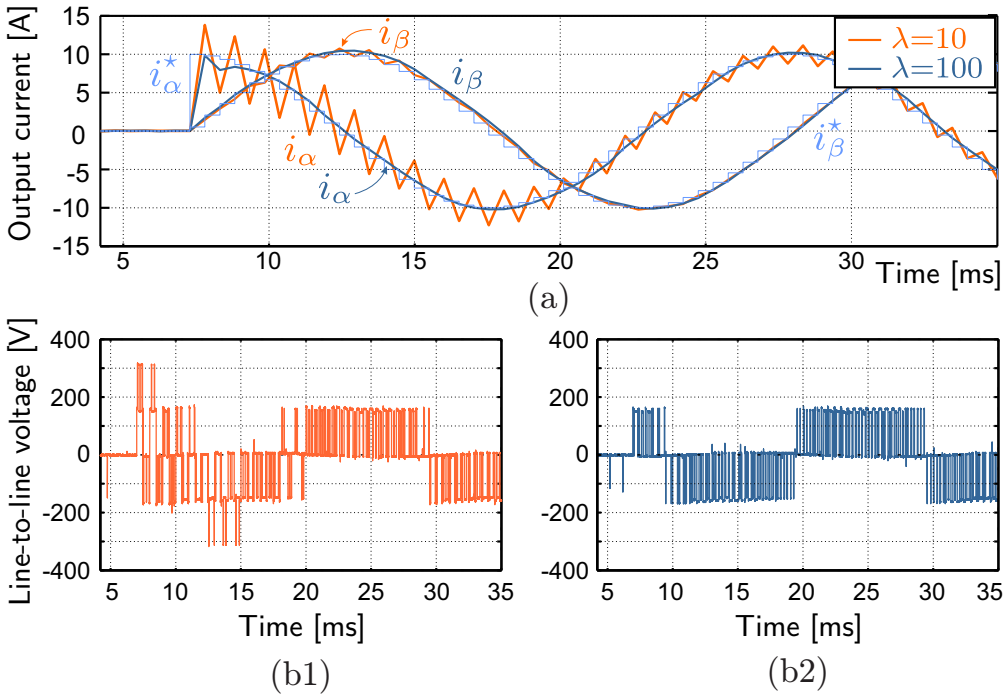


FIGURE 4.12: RL-Load: step response $\|i^{\star}\|= 0 \rightarrow 10$A for $\lambda=\{10, 100\}$: (a) $\alpha\beta$ currents and; line-to-line voltage for $\lambda=10$ (b1) and $\lambda=100$ (b2).

constant which indirectly shows that the capacitor voltages are balanced.

The harmonic spectra for the output current, phase and line-to-line voltages are shown in Fig. 4.11 when the modulation indexes of $m=\{0.54,\ 0.68,\ 0.89\}$ are utilised. It is shown in these graphics that the inverter phase voltage contains switching harmonics at f_s=2kHz and also 3rd harmonics with amplitudes of around 25% of the fundamental when large modulation indexes are used. As shown in Fig. 4.11, the third harmonics are eliminated from the line-to-line output voltages and also from the output currents. The dominant harmonics for the currents are 5th and 7th as shown in the top graphic of Fig. 4.11 .

Additionally, Fig. 4.12 compares the dynamic behavior of the controlled system for two different tuning parameters when a step change in the amplitude of the current reference, from 0 to 10A, is applied. As depicted in Fig. 4.12, a lower value of λ_{u} produces a very aggressive and oscillatory dynamic response, which degrades the controlled system performance.

4.5 Cascaded-OSS Model Predictive Current Control

The performance of the proposed MPC strategy for current control when the 3L-NPC converter is connected into the grid is evaluated in this section. As shown in Table 4.3, the dc-link voltage and rms value of the grid voltage are set, respectively, as V_{dc}=150V and V_{rms}=50V. The switching cycle is T_{s}=300 μs. For a better visualization of the main variables, the current and the voltage

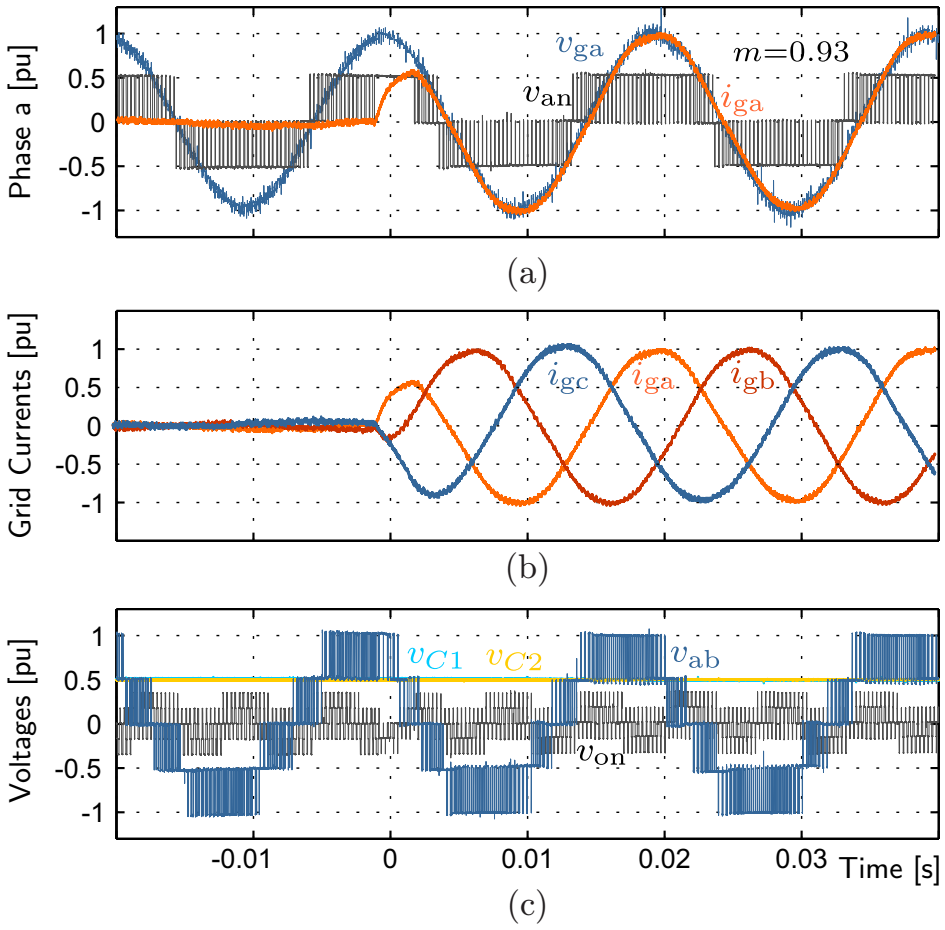


FIGURE 4.13: Cascaded-OSS-MP-CC: experimental waveforms under a step change in the amplitude of the grid current at unity power factor (PF=1) with λ=100: (a) phase a variables; (b) abc grid currents and; (c) converter voltages (pu. of $V_{\rm dc}$)

of the grid are normalised respect to their maximum amplitudes (10A and $50\sqrt{2}$V, respectively), meanwhile the inverter voltages are referred to the dc-link voltage (150V).

Fig. 4.13 shows the dynamic response of the controlled system when the amplitude of the grid current is step-changed from 0.5 to 10A maintaining unity power factor operation. Fig. 4.13(a) shows a fast dynamic response without overshoot of the grid current i_{ga}, maintaining a zero degree phase-shift respect to the grid voltage v_{ga}. The three-phase currents are sinusoidal without any

TABLE 4.3: Main Converter and Controller Parameters.

Parameter	RL-load	Grid-Connected	
		OSS-MP-CC	OSS-MP-DPC
$V_{\rm dc}$	150 V	150 V	250 V
$V_{\rm g}$	0 V	70 V	120 V
$T_{\rm s}$	500 μs	300 μs	300 μs

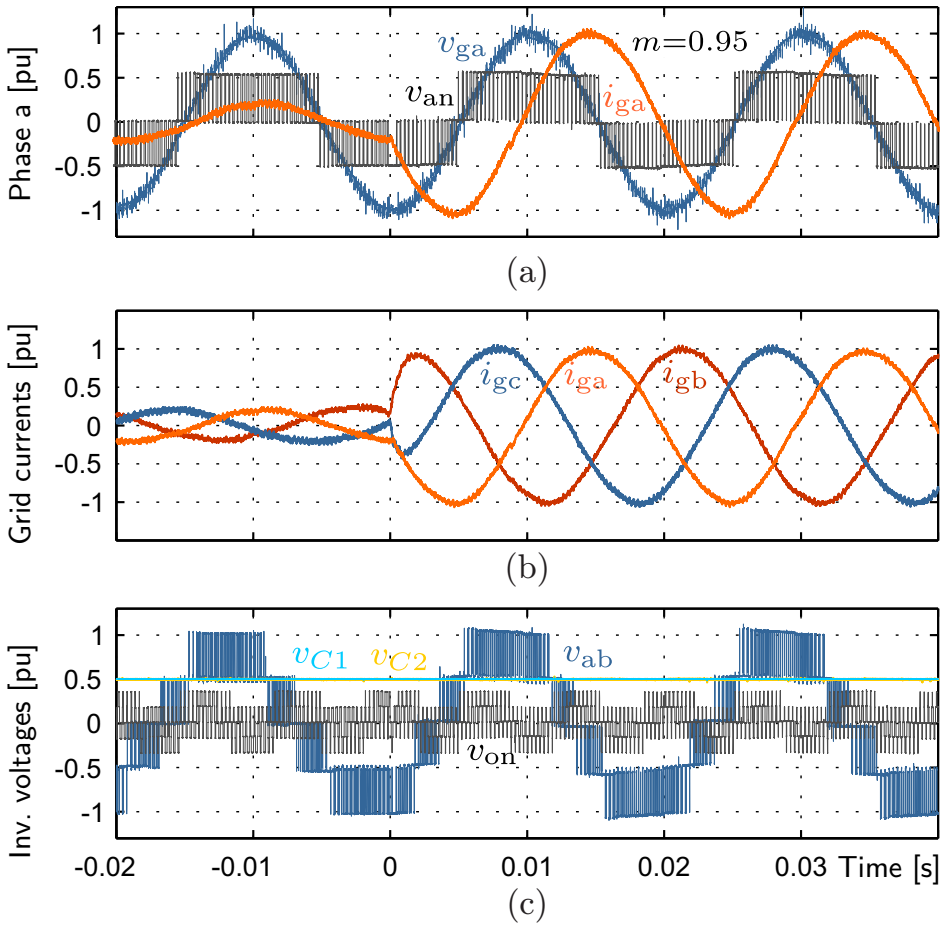


FIGURE 4.14: Cascaded-OSS-MP-CC: Experimental waveforms under a step change in the amplitude of the grid current at PF = 0.2 with λ_{u}=100: (a) phase a variables; (b) abc grid currents and; (c) converter voltages (pu. of V_{dc}).

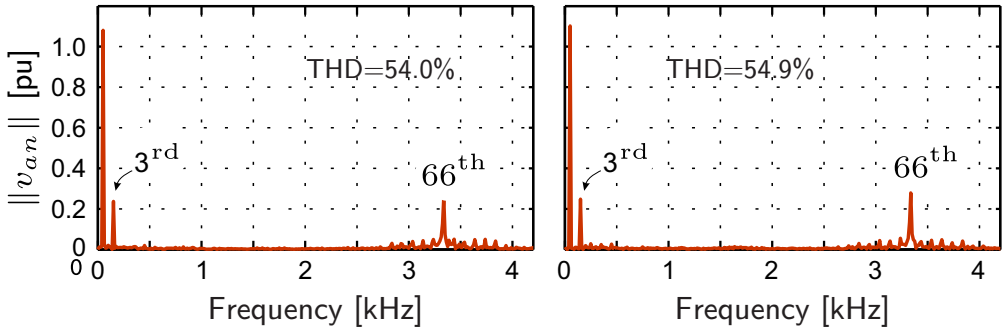


FIGURE 4.15: Cascaded-OSS-MP-CC: harmonic spectrum of inverter voltages (in pu of $V_{\mathrm{dc}}/2$) for two power factor (PF) conditions; (a) PF = 1.0; (b) PF = 0.20.

noticeable distortion, as depicted in Fig. 4.13(b). As shown in Fig. 4.13(c), the inverter line-to-line voltage (in pu of V_{dc}) has five levels meanwhile the capacitor voltages are well balanced. Moreover, the maximum common-mode voltage is $V_{\mathrm{dc}}/3$, which is the typical value obtained when a 7S-SS modulation pattern is applied [76].

On the other hand, Fig. 4.14 shows the performance of the controlled system when the converter is firstly injecting currents of amplitude 2.0A operating with unity power factor (i.e., $\boldsymbol{i}_{\mathrm{g}}^{\star}$=2+$j$0A). At t=0, the reactive current component of the grid current is step-increased in order to inject the maximum available reactive power achievable considering the capacity of the converter (i.e., $\boldsymbol{i}_{\mathrm{g}}^{\star}\approx$2+$j$9.68A). The resulting power factor is PF=0.2 meanwhile the dc-link capacitor voltages are well balanced as depicted in Fig. 4.14(c). This test shows the capability of the inner-MPC to balance the capacitor voltages even for low power factor operating conditions.

The harmonic spectrum of the inverter phase voltage v_{an} (in pu. of $V_{\mathrm{dc}}/2$) for both power factors is shown in Fig. 4.15. As shown in this graphic, a dominant third harmonic with an amplitude of approximately of 0.25 pu. is present in both cases. This is a zero sequence harmonic and as such it is not present in the line-to-line voltages. Besides, a harmonic component appears at f_s=3.3kHz, which is approximately, twice the device switching frequency.

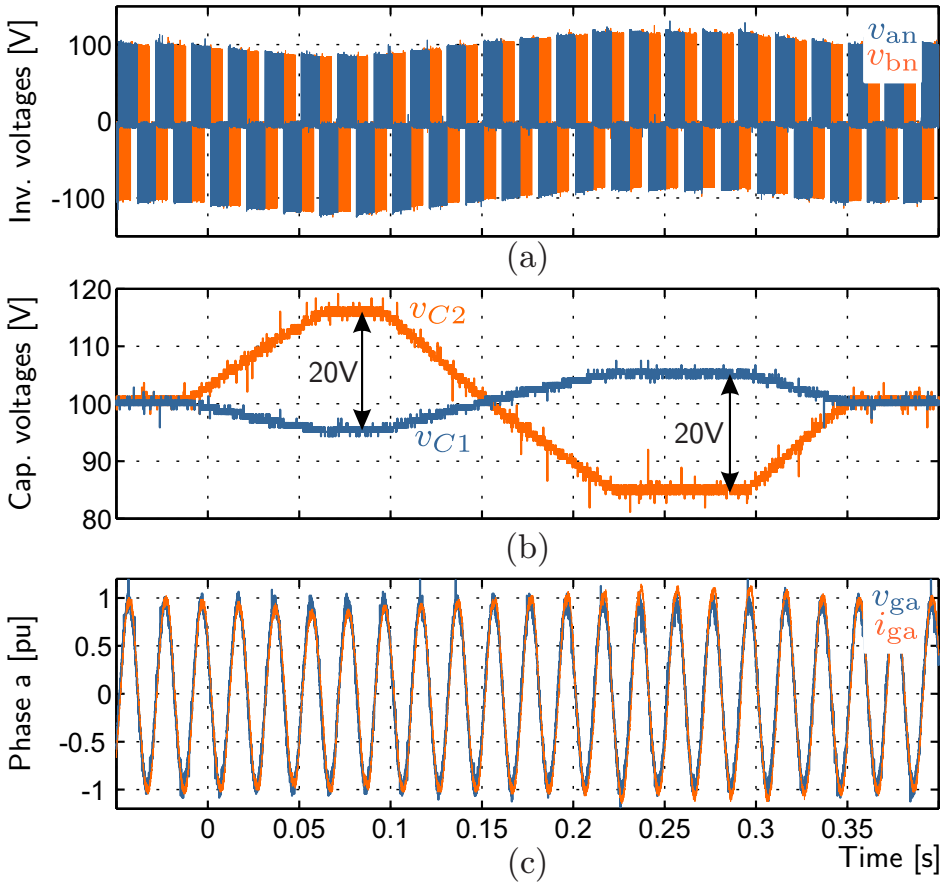


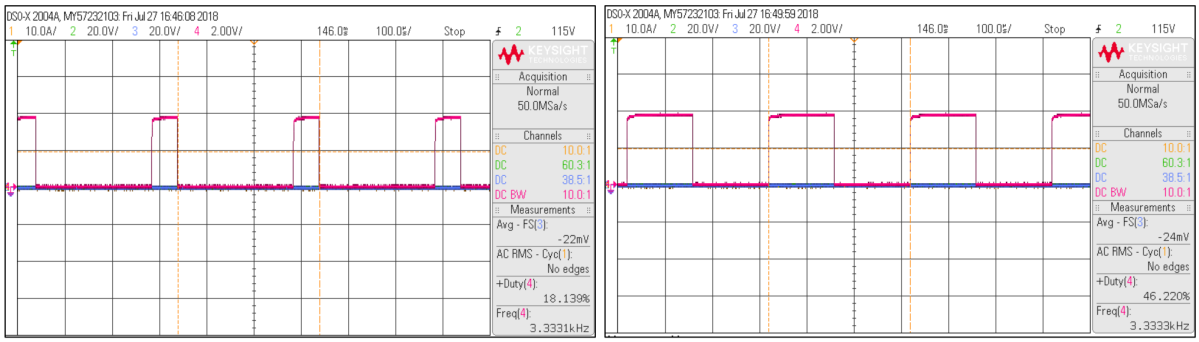
FIGURE 4.16: Cascaded-OSS-MP-DPC: experimental waveforms of the grid-connected configuration under step changes in the NP-voltage reference with λ=100: (a) Inverter phase voltages; (b) capacitor voltages and; (c) current and voltage of the grid in phase a.

4.5.1 Inner-MPC

Finally, to explore the effectiveness of the proposed Inner-MPC algorithm, the NP-voltage reference is sequentially changed using the following voltage values $v_{\mathrm{n}}^{*}=\{0, 20, -20, 0\}\mathrm{V}$ considering nominal apparent power and unity power factor. From the experimental waveforms presented in Fig. 4.16, it is concluded that the voltage difference in the capacitor voltages tracks the imposed references maintaining a good regulation of the grid current even when the assumption $v_{\mathrm{n}} = 0$ is not fulfilled.

4.5.2 Evaluation of the Computational Burden

One of the major concerns about MPC algorithms is the computational cost. To evaluate the computational burden of the proposed C-OSS-MPC, its execution time has been measured. As shown in Fig. 4.17(a), the time required to perform all the calculations is 54.3 μs, which corresponds to the 18.1% of the available time. On the other hand, when the controller is performed by using an enumeration search algorithm over the 24 regions, the execution time increases up to 138.7 μs, as depicted in Fig. 4.17(b). Therefore, the proposed control algorithm, illustrated in Fig. 3.6, allows reducing the computational burden in almost 61%.



(a) (b)

FIGURE 4.17: Execution time of the control strategies: (a) Proposed C-OSS-MPC algorithm shown in Fig. 3.6, and (b) C-OSS-MPC algorithm evaluating the 24 regions using a enumeration algorithm.

4.6 Cascaded-OSS Model Predictive Direct Power Control

In this section, the performance of the C-OSS-MPC for direct power control of grid-connected 3L-NPC converters (see section 3.7) is evaluated in this section. The block diagram of the control system is shown in Fig. 4.18.

As indicated in Table 4.3, the dc-link voltage and the amplitude of the grid voltage are set, respectively, as $V_{\rm dc}$=250V and $V_{\rm g}$=120V. The switching cycle is T_s=300 μs. For a better visualization of the main variables, the current and the voltage of the grid are normalized respect to their maximum amplitudes considering a rated apparent power of 2kVA, meanwhile the inverter voltages are referred to the half of the dc-link voltage (125V).

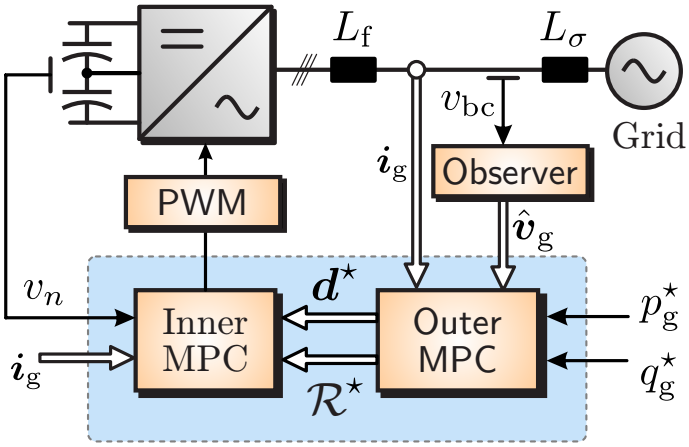


FIGURE 4.18: Proposed C-OSS-MPC for direct power control.

4.6.1 Comparison of prediction models

The first test compares the controlled system responses when two prediction models are implemented. The first one utilizes the prediction of the instantaneous active and reactive powers at the end of the switching period (i.e., $\boldsymbol{x}_p(k{+}1) = \boldsymbol{x}_{p8}$ in Fig. 3.4) [62]. The second one is the proposed prediction model that makes use of the average trajectory (i.e., $\boldsymbol{x}_p(k{+}1) = \boldsymbol{x}_{p4}$ in Fig. 3.4).

Fig. 4.19 compares the behaviour of the controlled system for both cases of study when a step change in the amplitude of the active power reference, from 0 to 0.75 pu (1.5 kW) is applied with unity power factor. As depicted in Fig. 4.19, the proposed prediction model (blue colour waveforms) produces the same dynamic response with an improved steady-state tracking error (cf. [38,86]). This experimentally shows that the proposed discrete-time model based on the average trajectory achieves a better performance than the standard one based on the instantaneous value at the end of the sampling period.

Additionally, the inverter voltages, the current and voltage waveforms at the PCC are shown in Fig. 4.20 for these two prediction models. It is observed that, in both cases, the estimated grid-

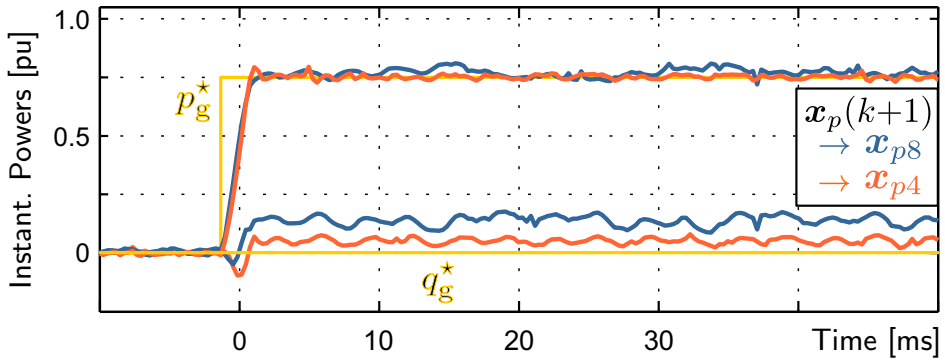


FIGURE 4.19: Cascaded-OSS-MP-DPC: effect of the prediction model on the system response to an instantaneous active power command step $p_g^\star = 0 \rightarrow 0.75$pu.

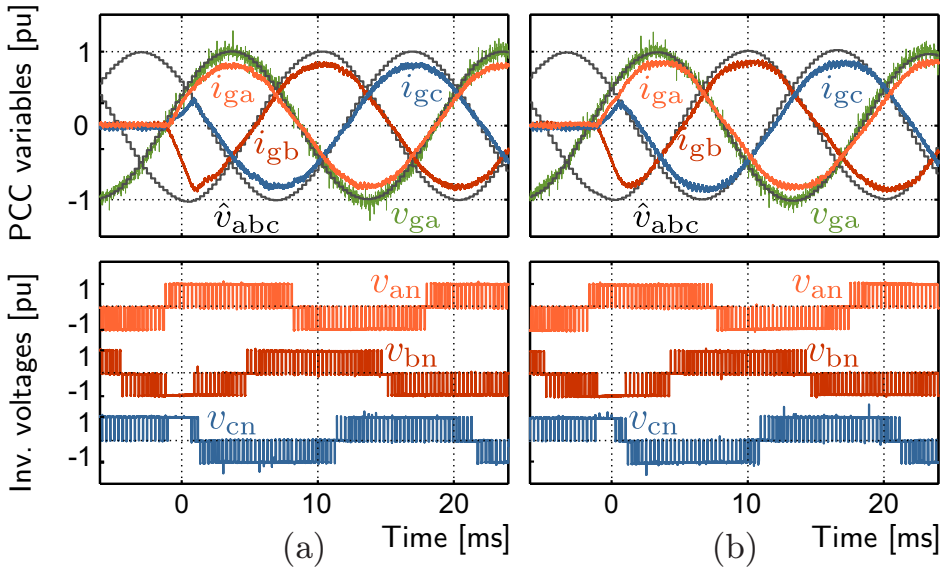


FIGURE 4.20: Cascaded-OSS-MP-DPC: experimental waveforms for the two cases shown in Fig. 4.19 (a) at the end of the sub-cycle and; (b) at the en of the switching cycle.

voltage is, in essence, the filtered version of the actual grid voltage. This can be clearly noted when comparing both phase-a voltages, i.e., v_{ga} (green line colour) versus the first component of $\hat{v}_{abc}$ (black lines colour).

4.6.2 Delay Compensation

The implementation of the control algorithm on a digital platform introduces a delay in the control action which deteriorates the closed-loop performance of the system [4]. However, in the case of MPC strategies, this problem can be overcome when a two-step ahead prediction is implemented, in which the variables to be controlled have to be firstly estimated at instant $k+1$ [87]. Then, in the second step, the prediction model (3.10) makes use of this prediction $\boldsymbol{x}_p(k+1)$ to evaluate the state variables at the next sampling instant $\boldsymbol{x}_p(k+2)$ over the set of feasible control actions.

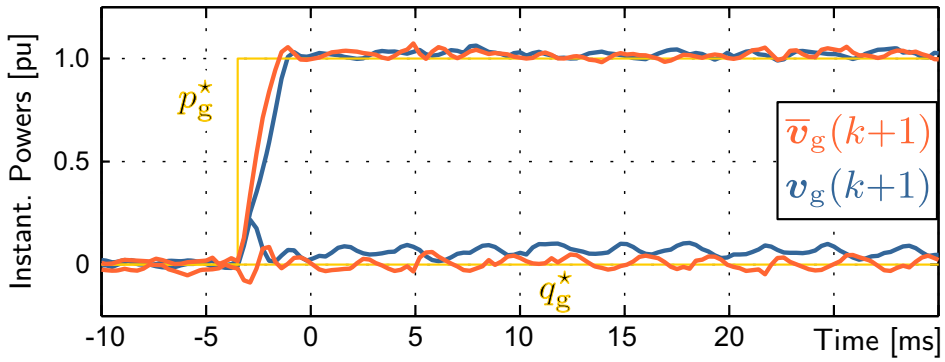


FIGURE 4.21: Cascaded-OSS-MP-DPC: effect of the grid-voltage prediction $\hat{v}_g(k+1)$ on the system response to an instantaneous active power command step $p_g^\star{=}0{\rightarrow}1.0$pu.

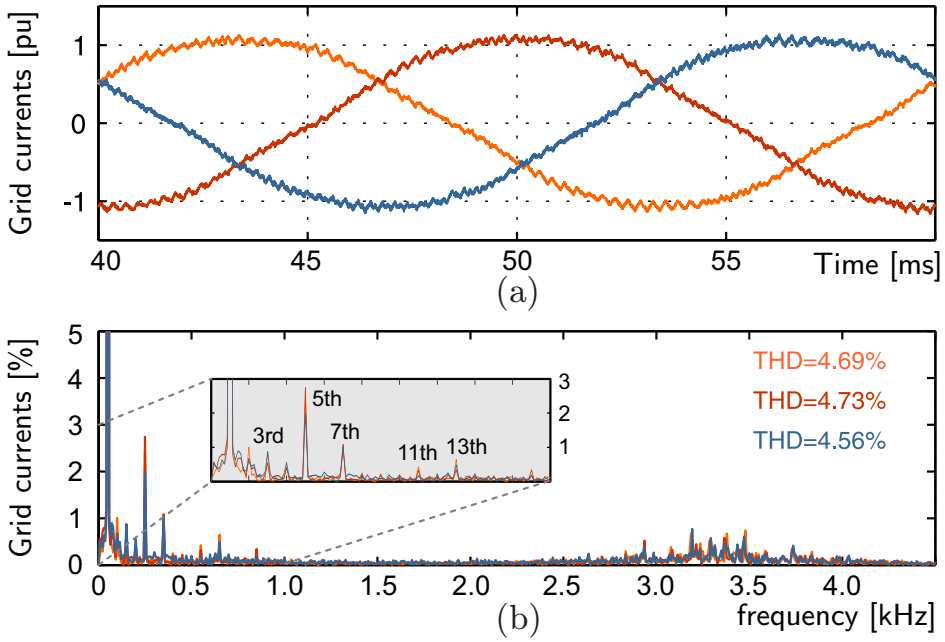


FIGURE 4.22: Cascaded-OSS-MP-DPC: grid currents during steady-state condition of Fig. 4.21: (a) waveforms and; (b) harmonic spectrum.

Because the OSS and the dwell-times of its SVs are known, in the first prediction step, the value of the instantaneous active and reactive powers at instant $k{+}1$ can be updated by sequentially employing the first-order discretization of (3.42). Instead, in this work, the discrete-time model is utilised by evaluating (3.10) with the average value of both the switching vector and the grid-voltage between the instants k and $k{+}1$ (notice that $\boldsymbol{\eta}(k)$ and $\boldsymbol{B}(k)$ in (3.44) depend on $\boldsymbol{v}_g$). The first one is directly obtained from the OASV computed in the previous sampling period $\boldsymbol{u}^\star(k{-}1)$ meanwhile the second one is calculated by using the information obtained from the GVO as:

$$\overline{\boldsymbol{v}}_g(k) = \frac{1}{2}\big(\hat{\boldsymbol{v}}_g(k{+}1) + \hat{\boldsymbol{v}}_g(k)\big). \tag{4.8}$$

In the same manner, the second prediction step is done by evaluating (3.10) with $\hat{\boldsymbol{x}}_p(k{+}1)$, $\boldsymbol{\eta}_0(k{+}1)$

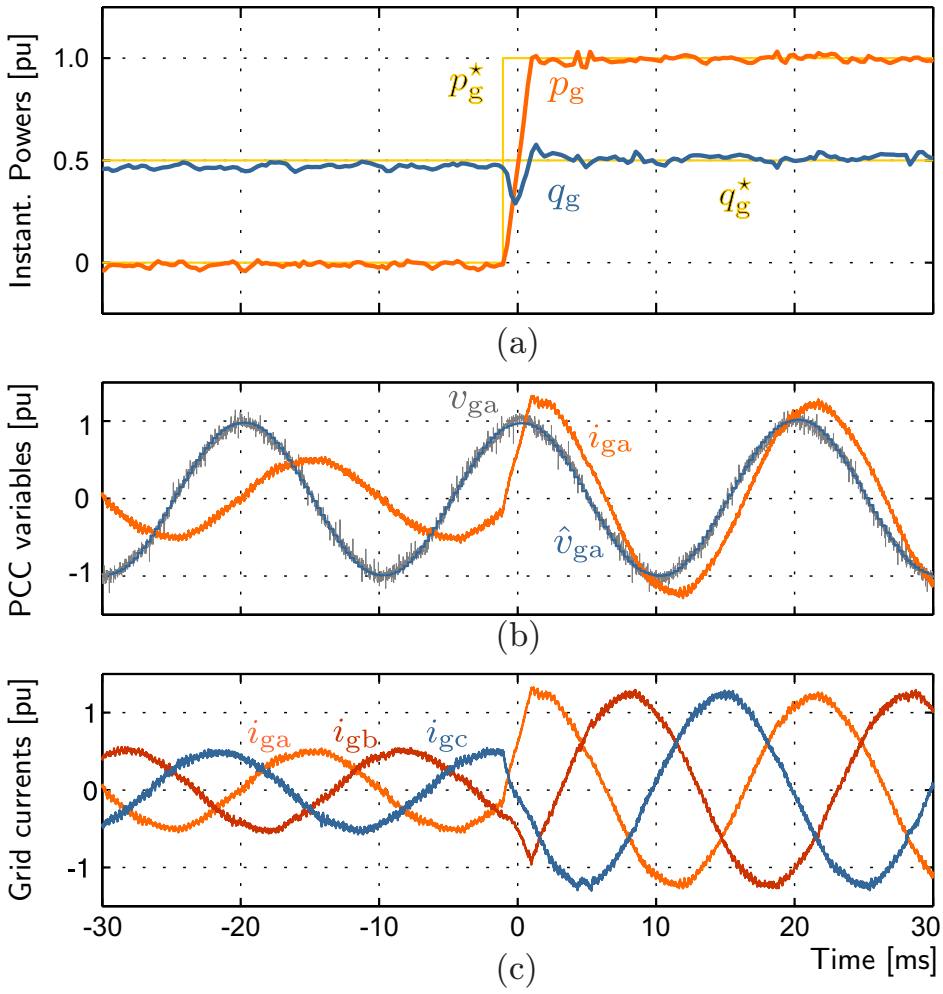


FIGURE 4.23: Cascaded-OSS-MP-DPC: experimental waveforms under a step change in active power reference: (a) instantaneous active and reactive powers; (b) phase a variables and; (c) abc grid currents.

and, $\boldsymbol{B}_0(k{+}1)$. These matrices are computed by using the mean value of the grid-voltage between the instants $k{+}1$ and $k{+}2$, which can be approximately predicted as

$$\overline{\boldsymbol{v}}_g(k{+}1) \cong \begin{bmatrix} \cos(T_0\omega_g) & -\sin(T_0\omega_g) \\ \sin(T_0\omega_g) & \cos(T_0\omega_g) \end{bmatrix} \hat{\boldsymbol{v}}_g(k{+}1) \tag{4.9}$$

Fig. 4.21 presents the performance comparison of the controlled system when the algorithm is implemented with the sampled and the average grid-voltage vector to evaluate the delay compensation. Dynamically, in both cases, the controller behaves correctly. However, when the average tracking error of the active and reactive powers are analysed, it shows that, using the average grid-voltage, they are reduced from 2.18% to 1.74% and from 6.48% to 0.67%, respectively. According to this result, hereinafter the average value is used instead of the sampled value of the grid-voltage vector.

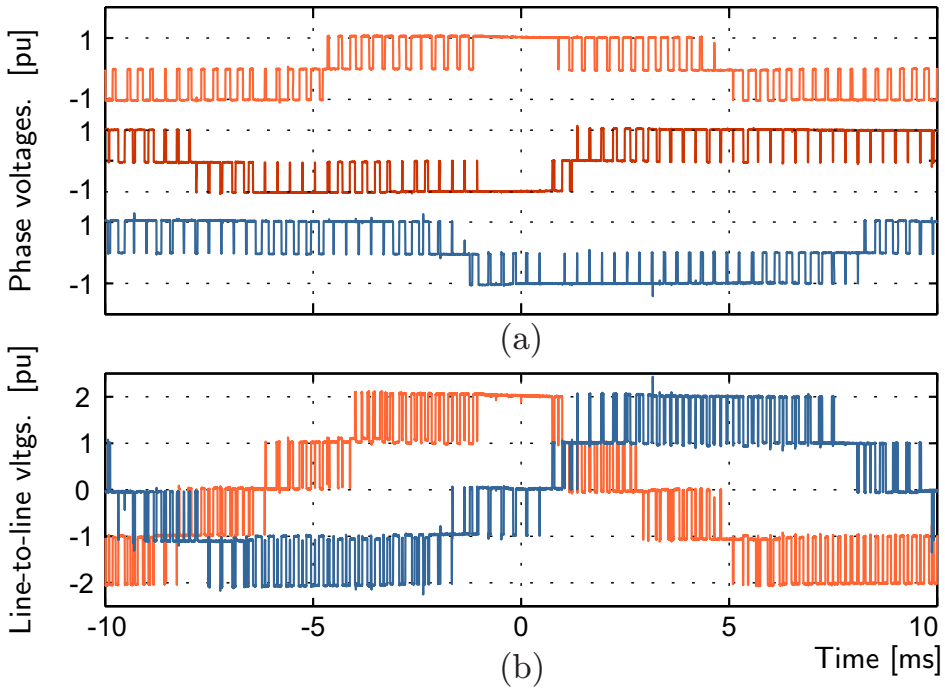


FIGURE 4.24: Cascaded-OSS-MP-DPC: experimental waveforms of converter voltages during the step-change shown in Fig. 4.23.

Additionally, Fig. 4.22 shows the steady-state performance of the grid currents operating with full power and unity power factor $p_{\mathrm{g}}^{\star}$=1 pu. (2kW). From the harmonic spectra depicted in Fig. 4.22(b), it is observed that a shaped harmonic spectrum is imposed by the control system where the amplitude of the harmonic components are below 3% achieving a very low THD for the three-phase currents (4.66% average). The high frequency components are around the switching cycle frequency given by $f_{\mathrm{s}} = 1/T_{\mathrm{s}} = 3.3$kHz.

On the other hand, Fig. 4.23 shows the performance of the controlled system when the converter is firstly injecting reactive power of 1 kVar ($q_{\mathrm{g}}^{\star} = 0.5$ pu.) and the active power reference is suddenly

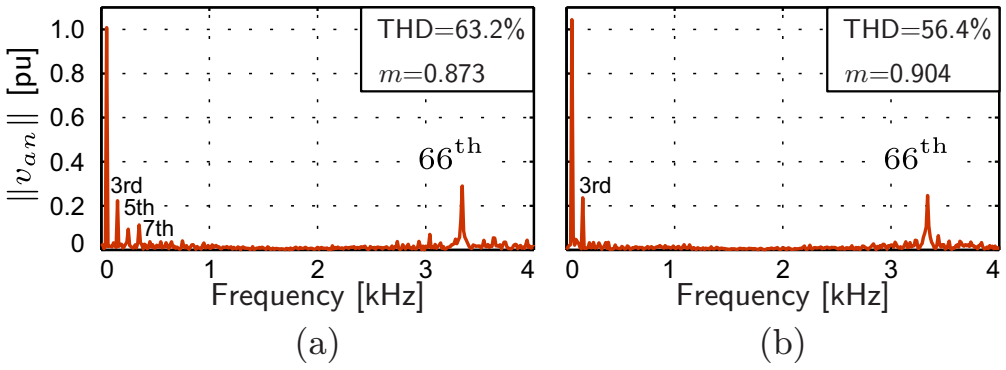


FIGURE 4.25: Cascaded-OSS-MP-DPC: harmonic spectrum of inverter voltages (in pu of $V_{\mathrm{dc}}/2$) for two power factor (PF) conditions; (a) PF = 0.0; (b) PF = 0.89.

changed from $p_{\mathrm{g}}^{\star}$=0 to $p_{\mathrm{g}}^{\star}$=1 pu. Fig. 4.23(a) shows a fast dynamic response without overshoot of the active power p_{g} meanwhile a relatively large disturbance is observed in the reactive power response. The resulting three-phase currents are depicted in Fig. 4.23(b). As shown in Fig. 4.24, the inverter voltages (referred respect to $V_{\mathrm{dc}}/2$) presents 3 levels and the line-to-line voltages has 5 levels. It is important to highlight that the differences between adjacent voltage levels are constant, as depicted in Fig. 4.24(a), which indirectly demonstrates that the converter is operating with the capacitor voltages balanced. This test proves the capability of the proposed Cascaded-OSS-MPC strategy to balance the converter even for zero power factor operating conditions.

Fig. 4.25 shows the harmonic spectrum of the inverter voltages for the two operating conditions depicted in Fig. 4.23 [(a) when the converter is only injecting reactive power of 1 kVar (PF = 0); (b) then when the active power is 2kW (PF=0.89)]. As shown in Fig. 4.25, the inverter voltages has a dominant third harmonic of an amplitude of approximately of 0.25 pu (similar to open-loop operation using SVM [76]). Moreover, a high-frequency harmonic component appears at 3.3 kHz, which is approximately, twice the power devices switching frequency. The THD is reduced in almost 10% when the converter is injecting rated active power.

4.6.3 Inner-MPC

Finally, to investigate the effectiveness of the proposed CVB strategy, the NP-voltage reference is changed as $v_{\mathrm{n}}^{\star} = \{0, 25, 0\}$V. From the experimental waveforms presented in Fig. 4.26, it is concluded that the voltage difference in the capacitor voltages tracks the imposed set points maintaining an acceptable regulation of the grid current.

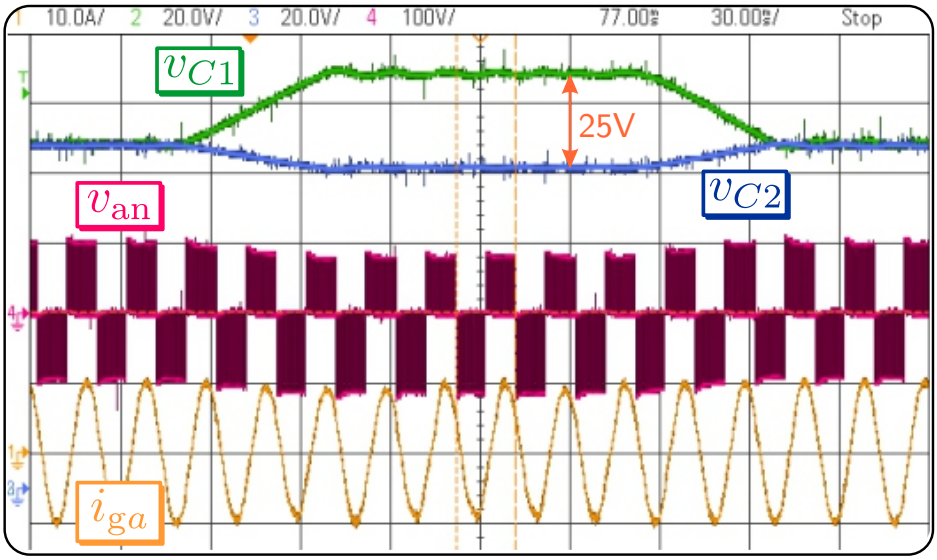


FIGURE 4.26: NP-voltage response under two step changes.

CHAPTER 5

Conclusions and Future Work

5.1 Conclusions

In the last years, the integration of distributed energy resources into electric power systems has been emerging as a critical issue driven by environmental motivations and economical stimulus. This fact has imposed technical and technological significant challenges concerning reliability, stability and electric power quality. Under this perspective, the impact of grid-connected voltage source converters becomes more significant.

Owing to the experimental results obtained in this thesis project, it can be stated that the proposed Cascaded-OSS-MPC strategy can be successfully applied for grid-connected power converter applications. Additionally the major finding of this PhD project are discussed below.

In this thesis project, two Cascaded OSS-MPC strategies for grid-connected three-level NPC converters have been proposed. The first one was designed for grid-current control and the second one for directly controlling the active and reactive powers injected at the PCC.

The proposed strategy introduces two well-formulated control optimal problems to optimally achieve the primary control goal (current or power control) and the balancing of the capacitor voltages avoiding all the problems and difficulties related to the weighting factors design. On the one hand, the Outer-MPC provides the optimal modulation region along with its duty cycles for establishing the optimal switching sequence which minimizes the average tracking error during each switching period. According to its structure, the Inner-MPC stage can be extended for two-level voltage sources converters.

On the other hand, the Inner-MPC determines the optimal dwell-time distribution of the small-size switching vectors to balancing the capacitor voltages of the 3L-NPC converter. Moreover, it is possible to regulate the closed-loop bandwidth of the outer controller by adding an extra term to the respective cost function that penalizes the control input effort.

Furthermore, the proposed Cascaded-OSS-MPC only evaluates 3 of the 24 regions of the hexagon in every sampling period, and thus its computational burden is reduced in comparison with standard OSS-MPC strategies that evaluate the cost function for all the modulation regions.

Extensive simulation and experimental tests presented in this work have demonstrated that the proposed methodology achieves good performance in both steady state and dynamic operation.

The resulting MPC strategy allows the converter to operate with a well-defined output voltage spectrum with most of the harmonic contents concentrated in the high-frequency range, relatively low and fixed switching frequency and, fast dynamic response during substantial reference changes. These results makes the proposed Cascaded-OSS-MPC strategy suitable for grid-connected power converter applications.

5.2 Summary of contributions

The contributions of this work can be summarised as follows:

- Two Model Predictive Control Strategies based on Optimal Switching Sequences are proposed to handle grid-connected 3L-NPC power converters.
- A comprehensive formulation of the proposed OSS-MPC strategy which embeds the modulation stage in the optimal control problem.
- The proposed control strategy takes advantage of the symmetric nature of the switching sequences to reduce the average tracking error during each switching cycle.
- The proposed Cascaded-OSS-MPC strategy introduces two well-formulated control optimal problems to optimally control both the primary control target (grid-current or active/reactive power) and the capacitor voltages balancing even during large disturbances and step-changes in the references.
- An efficient control algorithm is also addressed to reduce the computational burden typically observed in OSS-MPC strategies. Furthermore, the control algorithm can be extended and applied to other multilevel topologies.
- A very simple reduced order grid-voltage observer is introduced in this research effort to remove the distortion in the utility voltage waveform due to the high-frequency grid-current

ripple. This observer allows estimating the grid-voltage vector using just one voltage transducer.

- Experimental validation of the proposed control strategies is provided, including current control, direct active/reactive power control, and capacitor voltages. In all cases, the proposed Cascaded-OSS-MPC strategies perform excellent steady-state and transient response.

5.3 Future Work

The following are some interesting topics in which further research can be undertaken to extend the scope of this project:

- To implement the proposed OSS-MPC for 3L-NPC converters driving an induction machine introduced in the conference paper [88].

- Apply and extend the proposed OSS-MPC strategy to 4-Leg grid-connected power converters. In particular, aiming to define a computationally efficient control algorithm to enable the OSS-MPC strategy to be applied to 4-Leg 3L-NPC converters in which the number of control regions (tetrahedrons in this case) increases up to 192 [80].

CHAPTER 6

Publications

6.1 Papers related to the Ph.D work

6.1.1 Published Journal Papers

(J1) **A. Mora**, R. Cardenas, R. Aguilera, A. Angulo, F. Donoso, and J. Rodriguez, "Computationally Efficient Cascaded Optimal Switching Sequence MPC for Grid-Connected Three-Level NPC Converters," Accepted for publication to the *IEEE Transactions on Power Electronics*, 2019. **Q1**

(J2) **A. Mora**, M. Urrutia, R. Cardenas, A. Angulo, M. Diaz, M. Espinoza, and P. Lezana, "Model-Predictive-Control-Based Capacitor Voltage Balancing Strategies for Modular Multilevel Converters," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2432-2443, March 2019. **Q1**

(J3) F. Donoso, **A. Mora**, R. Cardenas, A. Angulo, D. Saez and M. Rivera, "Finite-Set Model-Predictive Control Strategies for a 3L-NPC Inverter Operating with Fixed Switching Frequency," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 5, pp. 3954-3965, May 2018. **Q1**

(J4) **A. Mora**, A. Orellana, J. Juliet and R. Cardenas, "Model Predictive Torque Control for Torque Ripple Compensation in Variable-Speed PMSMs," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4584-4592, July 2016. **Q1**

6.1.2 Under Review Journal Papers

(R1) **A. Mora**, R. Cardenas, R. Aguilera, A. Angulo, P. Lezana, and Dylan Lu, "Enhanced Predictive Direct Power Control for Grid-Connected 3L-NPC Converters.," in *IEEE Transactions on Industrial Electronics*, 2018. **Q1**

(R2) **A. Mora**, R. Cardenas, M. Urrutia, M. Diaz, and M. Espinoza, " A Power Control Strategy for 4-Leg Grid-Connected Inverters Operating Under Unbalanced Grid Voltage Conditions," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2018. **Q1**

6.1.3 Conference Papers

(C1) **A. Mora**, R. Aguilera, R. Cardenas, P. Lezana and Dylan D.C. Lu, "Phase-Shifted Model Predictive Control of a Three-Level Active NPC Converter," ISIE 2018, 27th International Symposium on Industrial Electronics, Cairns, Australia, June 12-15, 2018.

(C2) **A. Mora**, F. Donoso, M. Urrutia, A. Angulo and R. Cardenas, "Predictive Control Strategy for an Induction Machine fed by a 3L-NPC Converter with Fixed Switching Frequency and Improved Tracking Error," ISIE 2018, 27th International Symposium on Industrial Electronics, Cairns, Australia, June 12-15, 2018

(C3) M. Urrutia, **A. Mora**, A. Angulo, P. Lezana, R. Cardenas and M. Diaz, "A Novel Capacitor Voltage Balancing Strategy for Modular Multilevel Converters," SPEC 2017, 3rd Annual Southern Hemisphere Power Electronics Conference, Puerto Varas, Chile, 2017

(C4) **A. Mora**, R. Cardenas, M. Espinoza and M. Diaz, "Active power oscillation elimination in 4-leg grid-connected converters under unbalanced network conditions," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 2229-2234.

(C5) **A. Mora**, M. Espinoza, M. Diaz and R. Cardenas, "Model Predictive Control of Modular Multilevel Matrix Converter," 2015 IEEE 24th International Symposium on Industrial Electronics (ISIE), Buzios, 2015, pp. 1074-1079.

6.2 Participation other publications

6.2.1 Published Journal Papers

(J5) M. Diaz, R. Cardenas, M. Espinoza, F. Rojas, **A. Mora**, J. C. Clare and P. Wheeler, "Control of Wind Energy Conversion Systems Based on the Modular Multilevel Matrix Converter," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8799-8810, Nov. 2017. **Q1**

(J6) **A. Mora**, J. Juliet, A. Santander and P. Lezana, "Dead-Time and Semiconductor Voltage Drop Compensation for Cascaded H-Bridge Converters," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7833-7842, Dec. 2016. **Q1**

(J7) **A. Mora**, P. Lezana and J. Juliet, "Control Scheme for an Induction Motor Fed by a Cascade Multicell Converter Under Internal Fault," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 11, pp. 5948-5955, Nov. 2014. **Q1**

6.2.2 Under Review Journal Papers

(R3) M. Espinoza, R. Cardenas, F. Donoso, A. Letelier, **A. Mora**, E. Espina, "Modelling and Control of an MMC-Based Drive Considering Variable DC-Port Voltage", Submitted for publication to the *IEEE Transactions on Power Electronics.*

(R4) Diaz, Matias; Donoso, Felipe; Espinoza, Mauricio; Cardenas, Roberto; Wheeler, Patrick; **Mora, Andres**; Rojas, Felix, "Fault-Ride Through Control of Modular Multilevel Cascade Converters for Wind Energy Generation and Transmission Systems", Submitted for publication to the *IEEE Transactions on Industry Applications.*

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APPENDIX A

Appendices

A.1 Symmetrical Voltage Sequences

As is well known, due to the discrete nature of voltage source converters (VSCs) [72], the control region in the stationary $\alpha\beta$ frame can be divided in several sectors depending on the number of levels of the converter, e.g., for the 2L-VSC, the control region is commonly divided into six sectors, although more convex combinations of three canonical (or active) vector can be used. Obviously, when a multilevel converter is used, the number of sectors may increased significantly [89].

It should be remarked that each region is composed of a finite set of switching vectors, and the way in which these vectors are applied by the converter is named sequence (or path in the sense of the graph theory). Since each switching vector is defined by the switches states, each voltage sequence defines a corresponding pulse pattern in the output voltage.

A.1.1 Symmetrical Voltage Sequence Composed of Three SVs

For the sake of simplicity, let us consider that each SS is composed of three switching vectors. It follows that a symmetrical switching sequence is defined for all regions as follows

$$\boldsymbol{S}_j = \Big\{ \boldsymbol{v}_{1j}[t_1/2],\, \boldsymbol{v}_{2j}[t_2/2],\, \boldsymbol{v}_{3j}[t_3],\, \boldsymbol{v}_{2j}[t_2/2],\, \boldsymbol{v}_{1j}[t_1/2] \Big\} \tag{A.1}$$

where t_i, with $i \in \{1,\, 2,\, 3\}$, are the dwell times for each of the switching vectors.

We consider that the symmetrical voltage sequence (A.1) is applied by the power converter

during the whole switching cycle. Due to symmetrical reasons, the analysis is only done for the subcycle $T_0 = T_\mathrm{s}/2$. Under this point of view, the concatenated behavior of a LTI system can be derived from the following three equations:

$$\boldsymbol{x}_{1j} = \boldsymbol{x}_0 \ + (\boldsymbol{A}\boldsymbol{x}_0 \ + \boldsymbol{B}\boldsymbol{v}_{1j})\, d_{1j} T_0 \tag{A.2a}$$

$$\boldsymbol{x}_{2j} = \boldsymbol{x}_{1j} + (\boldsymbol{A}\boldsymbol{x}_{1j} + \boldsymbol{B}\boldsymbol{v}_{2j})\, d_{2j} T_0 \tag{A.2b}$$

$$\boldsymbol{x}_{3j} = \boldsymbol{x}_{2j} + (\boldsymbol{A}\boldsymbol{x}_{2j} + \boldsymbol{B}\boldsymbol{v}_{3j})\, d_{3j} T_0 \tag{A.2c}$$

where $\boldsymbol{x}_0$ is the system state at the beginning of the switching cycle.

Thereby, using (A.2), the system state at the end of the subcycle is determined by

$$\begin{aligned}\boldsymbol{x}_{3j} =&(\boldsymbol{I} + \boldsymbol{A}T_0)\, \boldsymbol{x}_0 + T_0 \boldsymbol{B}\boldsymbol{U}_j\, \boldsymbol{d}_j + T_0^2 \boldsymbol{A}^2 (d_{1j}d_{2j} + d_{1j}d_{3j} + d_{2j}d_{3j})\boldsymbol{x}_0 + T_0^3 \boldsymbol{A}^3 (d_{1j}d_{2j}d_{3j})\boldsymbol{x}_0 \ \ldots \\ &+ T_0^2 \boldsymbol{A}\boldsymbol{B}\big[(d_{1j}d_{2j} + d_{1j}d_{3j})\boldsymbol{v}_{1j} + d_{2j}d_{3j}\boldsymbol{v}_{2j}\big] + T_0^3 \boldsymbol{A}^{\boldsymbol{2}} \boldsymbol{B} (d_{1j}d_{2j}d_{3j})\boldsymbol{v}_{1j}\end{aligned} \tag{A.3}$$

It should be noted that the system (A.2) is linear in each argument (bilinear) and thus, the trajectory (A.3) is nonlinear in $\boldsymbol{d}_j$. However, it can be assumed as linear only considering the first two terms in (A.3), Hence, the system state at the end of the subcycle can be approximately assumed as follows:

$$\hat{\boldsymbol{x}}_{3j} = (\boldsymbol{I} + \boldsymbol{A}T_0)\, \boldsymbol{x}_0 + T_0 \boldsymbol{B}\boldsymbol{U}_j\, \boldsymbol{d}_j \tag{A.4}$$

The error of this linear approximation can then be stated as

$$\begin{aligned}\boldsymbol{e}_{3j} =&T_0^2 \boldsymbol{A}^2 (d_{1j}d_{2j} + d_{1j}d_{3j} + d_{2j}d_{3j})\boldsymbol{x}_k + T_0^3 \boldsymbol{A}^3 (d_{1j}d_{2j}d_{3j})\boldsymbol{x}_k \\ &+ T_0^2 \boldsymbol{A}\boldsymbol{B}\big[(d_{1j}d_{2j} + d_{1j}d_{3j})\boldsymbol{v}_{1j} + d_{2j}d_{3j}\boldsymbol{v}_{2j}\big] + T_0^3 \boldsymbol{A}^{\boldsymbol{2}} \boldsymbol{B} (d_{1j}d_{2j}d_{3j})\boldsymbol{v}_{1j}\end{aligned} \tag{A.5}$$

Furthermore, by considering that the duty cycles have to satisfy the following constrains

$$\begin{aligned}&\mathbb{1}^\intercal \boldsymbol{d}_j = 1 \\ &d_{ij} \in [0,\, 1],\end{aligned} \tag{A.6}$$

an upper bound of the error given in (A.5) can be found. It is expressed as

$$\boldsymbol{e}_{3,\max} = \frac{1}{3} T_0^2 \boldsymbol{A}^2 \boldsymbol{x}_k + \frac{1}{27} T_0^3 \boldsymbol{A}^3 \boldsymbol{x}_k + \frac{1}{9} T_0^2 \boldsymbol{A}\boldsymbol{B}\big[2\boldsymbol{v}_{1j} + \boldsymbol{v}_{2j}\big] + \frac{1}{27} T_0^3 \boldsymbol{A}^2 \boldsymbol{B}\boldsymbol{v}_{1j} \tag{A.7}$$

Therefore, by assuming that the state matrix $\boldsymbol{A}$ is diagonal (or diagonalizable) and Hurwitz, as in the case of a grid-connected power converter with a LR output filter [see (2.8)], it is straightforward to prove that the maximum error in (A.7) is negligible whenever the subcycle duration is less enough than the time constants of the natural modes of the system.

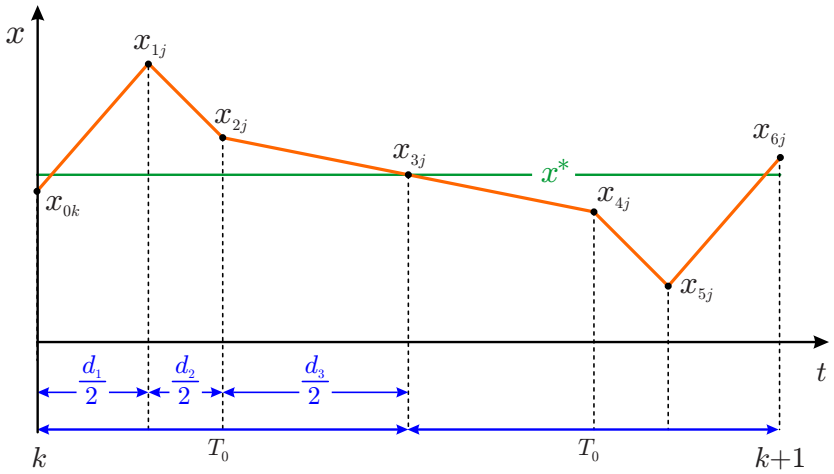


FIGURE A.1: Predicted system trajectories for a switching sequence of three switching vectors.

Therefore, if the switching frequency is high enough compared with system time constants, the dynamic evolution of the system state can be calculated considering $\boldsymbol{x}_{1j} \approx \boldsymbol{x}_{1j} \approx \boldsymbol{x}_k$. Thus, it can be assumed that it does not depend on the intersampling system state trajectory and then, the linear approximation in (A.4) will be considered.

Under this assumption, the system state at the end of the subcycle is determined by means of

$$\boldsymbol{x}_j[k{+}1] = (\boldsymbol{I} + \boldsymbol{A}T_0)\,\boldsymbol{x}[k] + \boldsymbol{F}_j\,\boldsymbol{d}_j, \tag{A.8}$$

where the matrix $\boldsymbol{F}_j \in \mathbb{R}^{n\times 3}$ is defined by the voltage vector sequence according to

$$\boldsymbol{F}_j = T_0\boldsymbol{B}\begin{bmatrix}\boldsymbol{v}_{1j} & \boldsymbol{v}_{2j} & \boldsymbol{v}_{3j}\end{bmatrix} \tag{A.9}$$

Based on (A.8), the system trajectory can be defined for each voltage sequence, and its corresponding final point $\boldsymbol{x}_j[k{+}1]$ is determined by the duty-cycle $\boldsymbol{d}_j$.

Remark 1 (Averaged Tracking Error).

The average trajectory during the whole sampling period is determined by definition as

$$\overline{\boldsymbol{x}} = \frac{1}{T_s}\int_{kT_s}^{kT_s+T_s} \boldsymbol{x}(t)dt \tag{A.10}$$

Assuming that a symmetrical voltage vector sequence is applied by the converter, the average

trajectory of the system can be approximated as

$$\overline{\boldsymbol{x}} = \frac{1}{4T_0}\Big[(\boldsymbol{x}_0+\boldsymbol{x}_1)\tau_1 + (\boldsymbol{x}_1+\boldsymbol{x}_2)\tau_2 + (\boldsymbol{x}_2+\boldsymbol{x}_3)\tau_3 + (\boldsymbol{x}_3+\boldsymbol{x}_4)\tau_3 + (\boldsymbol{x}_4+\boldsymbol{x}_5)\tau_2 + (\boldsymbol{x}_5+\boldsymbol{x}_6)\tau_1\Big] \tag{A.11}$$

Thereby, by replacing the system trajectory in the above equation, the trajectory of the system averaged over one sampling period (or switching cycle) is

$$\overline{\boldsymbol{x}}[k] = (\boldsymbol{I} + \boldsymbol{A}T_0)\boldsymbol{x}[k] + \boldsymbol{F}_j\,\boldsymbol{d}_j \;\; ; \tag{A.12}$$

which, according to (A.8)*, corresponds to the system state at the end of the subcycle, i.e.,*

$$\overline{\boldsymbol{x}}_j[k] = \boldsymbol{x}_j[k{+}1]. \tag{A.13}$$

Therefore, by using the OSS-MPC algorithm with symmetrical switching sequences, two of the main drawbacks of the OSV-MPC should be improved: the average steady-state error, and the variable switching frequency. Mathematically, this proves one of the key hypothesis of the proposed control algorithm.

It should be noted that the steady-state error decreases as the gap between the system state at the end of the subcycle $\boldsymbol{x}[k{+}1]$ and the reference system $\boldsymbol{x}^*$ decreases too. The degrees of freedom to meet with this control purpose are the duty-cycles in which the converter applies each switching vector belonging to a given switching sequence.

A.2 Experimental System

The description of the experimental set-up and converter prototype are introduced and briefly explained in this section.

The simplified diagram and the picture of the laboratory set-up for testing the proposed predictive control approach are depicted in Fig. A.2. As it is shown, a programmable DC power supply of 300 V and 10 A is used to provide the required dc-link voltage V_{dc}. Besides, a three-phase variac is connected to the secondary winding of a Dy1 power transformer. The variac is utilized to adjust the grid-voltage amplitude V_{g} whilst the power transformer is used to reduce the third order harmonic components at the PCC and also it provides isolation between the DC and AC sides.

A.2.1 Digital Platform

The control board based on digital signal processor TMS320C6713 DSP coupled with a XC3S400 FPGA is used in this research effort. Basically, it is composed of three different cards, as is depicted

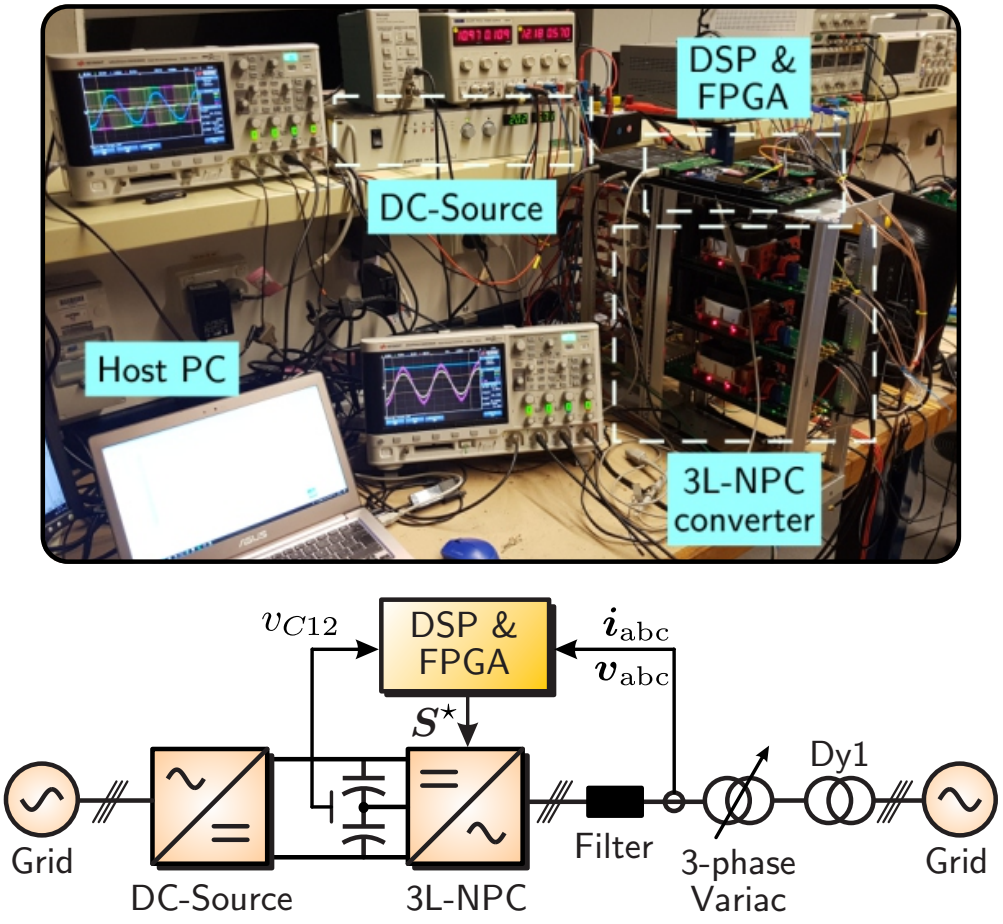


FIGURE A.2: Simplified laboratory setup.

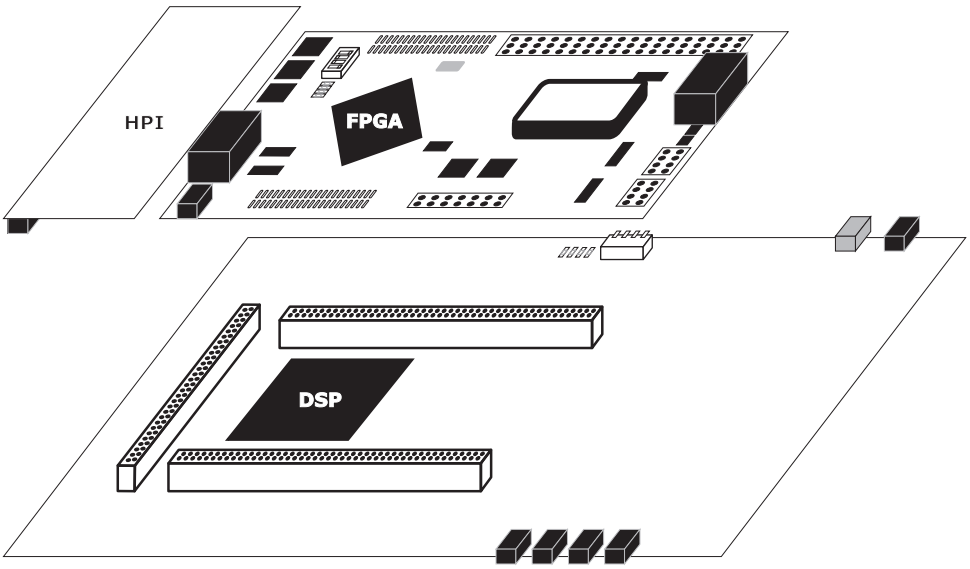


FIGURE A.3: Digital control platform scheme.

in Fig. A.3:

1. Peripherals board based on FPGA: this board controls all required peripherals for the PWM modulators and also the for two AD7266 analog-to-digital converters (ADCs). It is based on *Xilinx Spartan-3* XC3S400 FPGA.

2. Processing board based on DSP: this card is developed by *Spectrum Digital* and it is based on *Texas instrument* TMS320C6713 floating point DSP operating at 225 MHz with a 32-bits wide external memory interface.

3. PC communication card (HPI): this daughtercard allows serial, parallel and USB access to the DSP board. With this access an interface outside of Code Composer Studio (e.g. MATLAB) is provided.

A.2.2 The Three-Phase 3L-NPC Converter

A flexible three-phase 3L-NPC converter prototype was assembled in the University of Technology, Sydney Faculty of Engineering and Information Technology. This converter prototype was designed by Christina Poblete under the supervision of Dr. Aguilera.

Each converter leg is composed by four PCB boards which are interconnected with a mother-board PCB. Each module is shown in Fig. A.5 and a brief review of them is listed in the itemize bellow:

FIGURE A.4: Four assembly legs of the converter prototype.

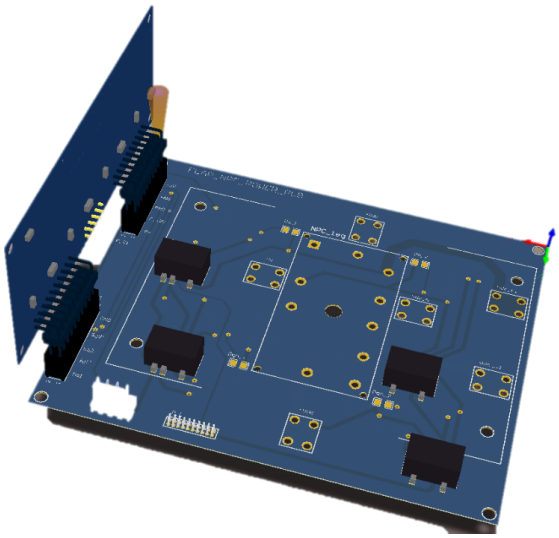
- The power PCB in which the Semikron Quad IGBT module SK20MLI066 (600 V and 30 A) as well the gate drivers were assembled [Fig. A.5(a)].

- The dead time and fiber optical transceiver PCB in which the gate signals s_{x1} and s_{x2} are received from the digital platform by fiber optic interface. In this board, the dead-time circuit provides the complementary gate signals $\bar{s}_{\mathrm{x1}}$ and $\bar{s}_{\mathrm{x2}}$ with the necessary inclusion of the dead time to avoid short-circuits of the dc-link capacitors (the measured dead time was 1.6μs). This board was designed in a horizontal position with the fibre optic transceiver connector, as shown in Fig. A.5(a).

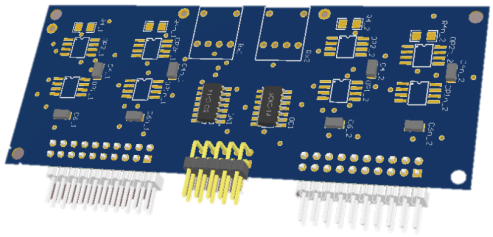
- The sensor PCB [Fig. A.5(c)] provides four sensors to allow measurement of the capacitor voltages v_{C12}, the inverter output voltage v_{xn} and current i_{x}. The measurement circuit for the inverter output voltage is based on a high-speed instrumentation amplifier of 15 MHz bandwidth and 22 V/μs slew rate.

- The DC-link PCB in which the two capacitors and 30 kΩ resistances were assembled.

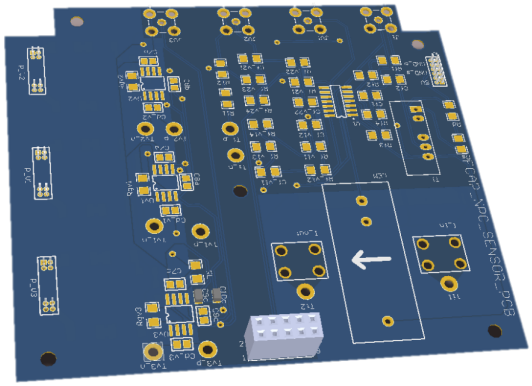
Fig. A.4 demonstrates how the final assembly looks like including the heat sink.



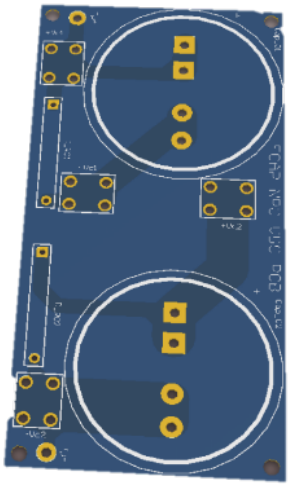
(A) Power and dead-time (DT) PCBs



(B) DT and fiber optical receiver PCB



(C) Sensor PCB



(D) DC-link PCB

FIGURE A.5: Designed PCB boards of the 3L-NPC converter prototype.