# Model-Predictive-Control-Based Capacitor Voltage Balancing Strategies for Modular Multilevel Converters

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***Abstract*—This paper presents two capacitor voltage balancing (CVB) strategies for modular multilevel converter (MMC) applications. Both balancing schemes are based on model predictive control and are designed to efficiently solve a constrained optimal control problem, where the predicted capacitor voltage errors are included in the cost function with the demanded output voltage of a cluster being forced through an equality constraint. The first method proposed in this paper computes specific modulation indexes for each module using the explicit solution of a relaxed version of the original optimization problem. The second approach proposed in this paper reduces the complexity of the original problem by linearizing the objective function and using an optimal sorting network based on a greedy algorithm to solve this approximation. Considering the structures of both solution approaches, they are integrated into modulation schemes based on phase-shifted and level-shifted pulsewidth modulation algorithms, respectively. Experimental results obtained from a nine-cell single-phase MMC prototype demonstrate the good performance achieved with the proposed methodologies, as well as the implementation simplicity offered by the proposed CVB algorithms.**

***Index Terms*—Floating capacitors, model predictive control (MPC), modular multilevel converters (MMCs), pulsewidth modulation (PWM).**

## I. Introduction

MODULAR multilevel converters (MMCs) are widely accepted technology with successful insertion in high-power and medium-voltage industrial applications. The high-quality output voltage signals; the possibility to reach higher voltage levels with lower rated semiconductors; the modular design, which allows redundancy and maintenance simplicity; their scalability without increasing the components rate; the option of using a transformerless configuration; and fault-tolerant operation capability are the most attractive features of these power converters [1]–[6].

The fundamental component of MMCs is the power cell, which is based on power semiconductors and a floating capacitor. These power cells are usually based on half- and full-bridge (see Fig. 1). The set of $n$ cells and an inductor connected in series constitute an arm (or branch), whose interconnections define specific topologies of MMCs family [3], [4]. For instance, the modular multilevel matrix converter (M3C) has two three-phase ac ports interconnected through nine arms as illustrated in Fig. 1(a). Another typical topology is the MMC (M2C) that is composed of six arms with half-bridge power cells, as shown in Fig. 1(c). Regarding applications, the MMC topologies have been applied to static synchronous compensators, high-power electrical drives, HVdc topologies, and wind energy conversion system [6]–[12]. The modulation methods for MMCs could be classified according to the switching frequency utilized. Within the high-frequency strategies, two conventional multicarrier pulsewidth modulations (PWMs) are typically used, phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM) [13]. On the other hand, one of the most practical and straightforward methods for low-switching frequency operation, especially for MMCs with a large number of cells, is the nearest level modulation (NLM) [4], [14].

The main challenge for the correct operation and control of MMCs is the voltage unbalancing produced in the floating capacitors of the converter. For an adequate operation of an MMC,

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it is essential to maintain the voltage of all capacitors within a feasible tolerance range. In this regard, several control strategies have been proposed in the literature where mainly the following aims are sought [15]–[18]: to control the total energy supplied to the converter; to balance the energy between all the arms; and to locally balance the energy of the cells located in a single arm. The latter is defined as capacitor voltage balancing (CVB) (or local balancing control) in this paper. Most of the CVB strategies discussed in the literature could be classified into two groups: 1) The CVB algorithms based on using additional voltage reference signals, which are consecutively synthesized by the modulation scheme (e.g., PS-PWM); and 2) the CVB algorithms that are somehow embedded in the modulation scheme (e.g., LS-PWM), which manipulate the switching state of each cell considering the cluster charging state and its capacitor voltages. [15]–[22].

For CVB purposes using PS-PWM, a proportional controller (PC) is included to locally balance the capacitor voltages [8], [18], [19]. In this method, the capacitor voltage is compared to its desired average value, and the resulting error is multiplied by the sign of the arm current and the controller gain to obtain a compensation signal. This signal is then added to the normalized reference voltage, thereby generating the modulation index for each cell. The dynamic and performance of this CVB strategy depends on the PC gain that can be adjusted using conventional linear control tools.

On the other hand, in [15] and [20], a priority list of cells is implemented by sorting the capacitor voltages of each cluster. In this strategy, the output voltage is built by modulating only one cell per period and keeping the rest of the cells either in the ON or OFF state during the full switching cycle. This CVB method utilizes the priority list and the charging/discharging cluster state to perform the voltage balancing. Moreover, it does not require the tuning of controller gains or other parameters; and thus, it is decoupled from the inner current control loop. However, this strategy can lead to an increased switching frequency [23] and undesired spikes in the cluster voltage [20]. To balance the capacitor voltages in low-switching frequency modulation strategies, as NLM, a CVB method is also required, which typically is based on sorting algorithms and a switching state designation stage [4], [14].

Recently, thanks to technological advances in microprocessors, the use of model predictive control (MPC) has been proposed for many applications related to power converters [24]. This control strategy can be applied to constrained nonlinear systems with multiple inputs and outputs (e.g., MMC) solving, at each sampling period, an optimal control problem (OCP) over a finite horizon [25], [26]. This paper proposes to use MPC for CVB in MMCs by using the state-average model of an $n$-cell cluster. The CVB problem is formulated as a single-period OCP (SP-OCP), from which two continuous control set MPC (CCS-MPC) strategies are derived. These algorithms are designed to solve two simplified versions of the underlying SP-OCP. The first one relaxes one of the constraints associated with the control inputs to produce a closed-form solution. This solution does not introduce a distortion into the output voltage, and its analytical structure allows embedding with the PS-PWM method.

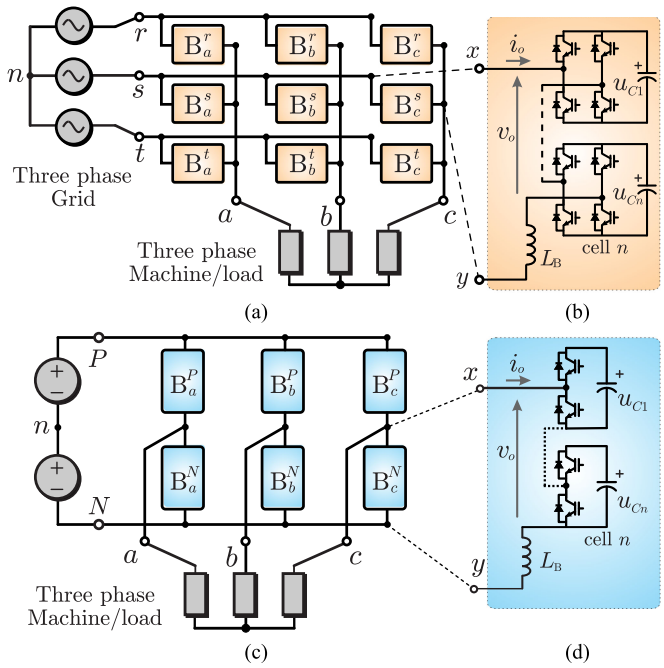


Fig. 1. MMC topologies: (a) M3C; (b) M2C; (c) arm based on full-bridge power cells; (d) arm based on half-bridge power cells.

The second MPC strategy proposed in this paper utilizes a linear approximation of the cost function, maintaining all its constraints. This primal formulation of the original SP-OCP is solved by using a greedy algorithm embedded with a sorting strategy of the capacitor voltages. The implementation of optimal sorting networks (OSN) [27] in field programmable gate arrays (FPGAs) is proposed in this paper to perform efficiently the process of building a priority list based on the capacitor voltage magnitudes.

The effectiveness of the proposed control strategies is validated through experimental results conducted with a nine module prototype rated to 5.6 kVA.

## II. CVB Strategies

The aims of the CVB strategy are to simultaneously control the mean value of each capacitor voltage and the output voltage (averaged over a switching cycle) generated by a cluster for a given current $i_o$. The typical structure of a cluster is depicted in Fig. 1(b), where $n$ full-bridge cells are connected in series.

For modeling purposes, it is considered that the $j$th capacitor has a capacity of $C_j$, a conductance $G_j$, and a voltage $u_{Cj}$. On the ac side of each cell, the voltage generated is $v_{oj}$, which instantaneously depends on the switching state $s_j \in \{-1, 0, 1\}$ and the capacitor voltage $u_{Cj}$. The set of all modules will be denoted as $\mathcal{C} = \{1, \ldots, n\}$, the reference voltage for the $j$th capacitor is $u^*_{Cj}$ and the desired output voltage to be modulated is $v^*_o$, which is typically defined by a current controller. Moreover, a switching time $T_s$ is assumed.

Considering the aforementioned, for each cluster, the capacitor balancing problem can be considered as a constrained OCP

defined as follows:

$$(\mathbf{P1}) \quad \min_{U_{Cj},m_j} \quad \sum_{j\in\mathcal{C}} \left(U_{Cj}-u^*_{Cj}\right)^2 \tag{1a}$$

$$\text{s.t.} \quad C_j\frac{\mathrm{d}U_{Cj}}{\mathrm{d}t}+G_jU_{Cj}=i_om_j \qquad \forall j\in\mathcal{C} \tag{1b}$$

$$\sum_{j\in\mathcal{C}} u_{Cj}m_j=v^*_o \tag{1c}$$

$$m_j\in[-1,1] \qquad \forall j\in\mathcal{C}. \tag{1d}$$

In this formulation, $m_j=\frac{1}{T_s}\int_0^{T_s} s_j(t)\mathrm{d}t$ is the $j$th modulation index, which is in the interval $[-1,1]$ for full-bridge cells, $U_{Cj}=\frac{1}{T_s}\int_0^{T_s} u_{Ck}(t)\mathrm{d}t$ is the $j$th capacitor voltage averaged over a switching cycle, and integrals over products between continuous variables and switching states are approximated by using first-order Taylor series around the point $(x,s)=(x(0),0)$ as $\frac{1}{T_s}\int_0^{T_s} x(t)\,s(t)\mathrm{d}t\simeq x(0)\,m$. Note that for MMCs based on half-bridges [see Fig. 1(d)], the switching states are defined as $s_j\in\{0,1\}$; and thus, $m_j$ belongs to the interval $[0,1]$.

In (**P1**), the capacitor voltage errors are considered in the quadratic cost function [see (1b)], whereas the other control target, i.e., generating the desired output average voltage $v^*_o$, is considered in the constraint (1c). This constraint means that $v^*_o$ has to be generated by a linear combination of the capacitor voltages weighted by the modulation indexes $m_j$. In addition, from the continuous-time model in (1b), it is concluded that for a given current $i_o$, the dynamic of the $j$th capacitor voltage $U_{Cj}$ depends on the modulation index assigned to the $j$th cell. Hence, all the control targets can be achieved by manipulating the modulation indexes of the cells.

To obtain the optimal control action $m_j$ for each cell, the problem (P1) can be reformulated by introducing the future value of $U_{Cj}$ in the cost function. For this purpose, the continuous-time model of the capacitor voltages in (1b) is discretized using Forward Euler, which leads to the following discrete-time model:

$$U_{Cj}[k+1]=\beta_jU_{Cj}[k]+\Delta\hat{u}_j[k]\,m_j[k] \tag{2}$$

with $\beta_j=1-\frac{T_sG_j}{C_j}$ and $\Delta\hat{u}_j[k]=\frac{T_s}{C_j}i_o[k]$, the maximum increment/decrement of the capacitor voltage when the maximum modulation index is applied to the cell. Consequently, the balancing capability is affected by the magnitude of the arm current at instant $t_k$, i.e., $i_o[k]$. Thus, by replacing (2) into the cost function in (1a), the SP-OCP is formulated as follows:

$$(\mathbf{P2}) \quad \min_{m_j[k]} \quad \sum_{j\in\mathcal{C}} \left(\beta_ju_{Cj}[k]-u^*_{Cj}[k]+\Delta\hat{u}_j[k]m_j[k]\right)^2 \tag{3a}$$

$$\text{s.t.} \quad \sum_{j\in\mathcal{C}} u_{Cj}[k]m_j[k]=v^*_o[k] \tag{3b}$$

$$m_j[k]\in[-1,1] \qquad \forall j\in\mathcal{C}. \tag{3c}$$

Notice that, according to its structure, the problem (**P2**) is known as a continuous quadratic knapsack problem [28] which can be solved in a real-time digital control system by using CCS-MPC [26].

Therefore, due to the limited processing time available for real-time control of power converters, two methodologies to reduce the complexity of (**P2**) are proposed in this research effort. The first method relaxes some constraints of this problem, preserving its original objective function (dual formulation), and the second one uses a linear approximation of the cost function, maintaining all its constraints (primal formulation).

In addition, hereinafter, it is assumed that the parameters and voltage references are equal for all cells, i.e., $\Delta\hat{u}_j[k]=\Delta\hat{u}[k]$, $\beta_j\simeq 1$, and $u^*_{Cj}[k]=U^*_C, \forall j\in\mathcal{C}$.

### A. Dual CVB Technique (Method-I)

The first approach to facilitate an approximated solution of (**P2**) is by ignoring the upper and lower limits of the control inputs [constraint (3c)]. Thereby, the solution is not necessarily feasible and a saturation scheme must be implemented.

Accordingly, the following dual formulation is derived:

$$(\mathbf{P2d}) \quad \max_{\lambda}\min_{|m_j|\le 1} \quad \sum_{j\in\mathcal{C}}\left(u_{Cj}[k]-U^*_C+\Delta\hat{u}_j[k]m_j[k]\right)^2 + \lambda\left(v^*_o[k]-\sum_{j\in\mathcal{C}}u_{Cj}[k]m_j[k]\right). \tag{4}$$

Since the inner problem of (**P2d**) is the sum of one–dimensional positive definite quadratic problems, its optimal solution is [29]:

$$m_j(\lambda)=\text{mid}\left\{-1,\ \frac{u_{Cj}[k]}{2\Delta\hat{u}[k]^2}\lambda+\frac{U^*_C-u_{Cj}[k]}{\Delta\hat{u}[k]},\ +1\right\} \tag{5}$$

where operator mid$\{\cdot\}$ defines the component-wise median.

On the other hand, the Karush–Kuhn–Tucker (KKT) conditions [30] of (**P2d**) are the constraint (3b), whose relaxed solution, when bounds over $m_j$ are ignored, is given by

$$\lambda=\frac{2\Delta\hat{u}[k]^2}{\sum_{j\in\mathcal{C}}u^2_{Cj}[k]}\left(v^*_o[k]-\frac{1}{\Delta\hat{u}[k]}\left(\sum_{j\in\mathcal{C}}U^*_Cu_{Cj}[k]-\sum_{j\in\mathcal{C}}u^2_{Cj}[k]\right)\right) \tag{6}$$

Therefore, the relaxed optimum of (**P2**) is finally obtained as follows:

$$m^*_j[k]=\frac{v^*_o[k]}{u_{\Sigma2}[k]}u_{Cj}[k]+\frac{U^*_C}{\Delta\hat{u}[k]}\left(1-u_{Cj}[k]\frac{u_{\Sigma1}[k]}{u_{\Sigma2}[k]}\right) \tag{7}$$

where $u_{\Sigma1}$ and $u_{\Sigma2}$ are, respectively, the linear and quadratic sum of the whole capacitor voltages, i.e.,

$$u_{\Sigma1}[k]=\sum_{i\in\mathcal{C}}u_{Ci}[k], \qquad u_{\Sigma2}[k]=\sum_{i\in\mathcal{C}}u^2_{Ci}[k]. \tag{8}$$

The structure of (7) does not allow us to define a proper modulation scheme at a glance. However, assuming that the capacitor voltages are well regulated with instantaneous values close to $U^*_C$, which is the desired steady-state operation, then $u_{\Sigma2}\simeq U^*_Cu_{\Sigma1}$; and thus, the relaxed optimal solution (7) can be assumed as follows:

$$m^*_j[k]\simeq m_0[k]+\left(\frac{1}{\Delta\hat{u}[k]}-\frac{m_0[k]}{U^*_C}\right)(U^*_C-u_{Cj}[k]) \tag{9}$$

being $m_0[k] = v_o^*/u_{\Sigma 1}$, the desired output voltage normalized by the available cluster voltage $u_{\Sigma 1}$.

As shown in (9), the approximated modulation index for each cell can be decomposed into two terms: the first one proportional to the desired output voltage $v_o^*$, and the second one commensurate with the capacitor voltage error. Hence, the optimal solution requires injecting a common modulation index to all modules $m_0[k]$ with a correction proportional to the capacitor voltage error. It follows that, under steady-state conditions, an almost even modulation index distribution among cells is established and, in consequence, the PS-PWM strategy is proposed to synthesize the output voltage when $m_j$ is computed according to (7) for all $j \in \mathcal{C}$. Therefore, the switching frequency harmonic cancellation, due to the phase shifting produced by the carrier, is accomplished and, the harmonic distortion of the output voltage can be minimized [13].

Unlike the CVB strategies introduced in [8], [18], and [19], one of the main advantages of (7) is the fact that it always satisfies the constraint (3b); thus, no voltage deviation on the synthesized voltage would be introduced by the converter and the output cluster voltage averaged over a switching cycle will be, ideally, equal to the reference voltage $v_o^*[k]$. However, depending on the reference updating method implemented for the PS-PWM [11], an additional source of distortion could be introduced by the converter.

### B. Primal CVB Technique (Method-II)

To reduce the complexity of the problem (**P2**), a linear approximation of its cost function is realised without ignoring any of the constraints. Thus, the solution will be feasible in the original domain.

A formal linear approximation of the cost function in (3a) is obtained by using the first-order Taylor representation around the origin. Thereby, and for minimization purposes, (**P2**) can be rewritten as follows:

$$(\mathbf{P2p}) \quad \min_{m_j} \quad -i_o[k]U_C^* \sum_{j\in\mathcal{C}} m_j[k]$$
$$\text{s.t.} \quad (3b) \text{ and } (3c). \tag{10}$$

This problem is a continuous linear knapsack with overall complexity $O(n)$. The optimal solution can be obtained using a greedy algorithm with a sorting strategy [31].

***1) Sorting Networks:*** FPGAs can be used to implement fast sorting networks due to its parallel computing capability. The parameters typically used to define the efficiency of the sorting algorithms are the size (number of comparisons required) and depth (number of stages) [27]. Among several methods, OSNs have been proposed in the literature where the number of comparators and stages are minimized for a given number of inputs [27], [32]. In the context of MMCs, the cluster capacitor voltages define the input set $\mathcal{U} = \{u_{C1}, \ldots, u_{Cn}\}$ for the sorting algorithm, whereas the indexes of the cell ordered from the maximum to the minimum voltage define its output set $\mathcal{N} = \{j_1, \ldots, j_n\}$. This set means that $u_{Cj_1} \geq \ldots \geq u_{Cj_n}$.

Fig. 2 shows the OSNs proposed in [27] for four, six, and nine inputs. Notice that 8 stages and 25 comparators (see Knuth notation in [27]) are necessary to sort 9 inputs, which in practice

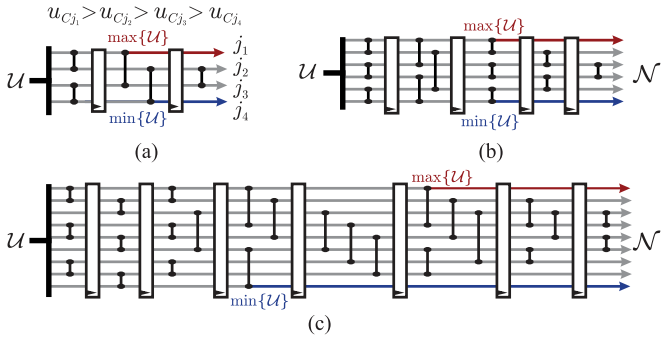


Fig. 2. OSNs with (a) four, (b) six, and (c) nine inputs [27].

would mean that eight main clock counts of the FPGA are necessary to obtain the fully sorted output set. In addition, it is worth noting here that, on contrary to sequential algorithms, the OSNs allow obtaining the min/max elements of $\mathcal{U}$ in fewer steps than those required to implement the full sorted set. This feature can be useful when a CVB strategy based on min/max elements is implemented [21], [22].

***2) Greedy Algorithm:*** In this strategy, all modulation indexes are initialized with $m = -1$ and going through the cells in increasing order of efficiency; every cell is switched to $m = 1$ until the first overshoot of the output voltage is caused in the $\ell$th iteration. Then, the execution of the algorithm is stopped and the modulation index of the cell that caused the overflow ($\ell$th cell) is computed to accomplish (3b), leading to

$$m_\ell = \frac{1}{u_{C\ell}} \left( v_o^* + \sum_{j=\ell+1}^{n} u_{Cj} - \sum_{j=1}^{\ell-1} u_{Cj} \right). \tag{11}$$

Taking into account the structure of (10), the cell efficiency is defined as follows:

$$\eta_j = -i_o[k]U_C^*/u_{Cj}[k]. \tag{12}$$

It follows that if $i_o < 0$, an increasing order of efficiency implies that the cells must be switched in decreasing order with respect to the capacitor voltage magnitudes. Conversely, when $i_o > 0$, the voltages are sorted in increasing order, and consequently, the cell with the lowest capacitor voltage magnitude will be the first to be switched from $m_j = -1$ to $m_j = 1$. Therefore, to obtain the optimal solution of (**P2p**) by using the greedy algorithm, the cells must be sorted according to their capacitor voltage magnitudes in increasing or decreasing order depending on the cluster current polarity.

It is worth to remark that transitions between $m = \pm 1$ allow some full bridges to be charged and others discharged in the same switching period, which, in general, will produce a fast balancing response but large capacitor voltages ripple. Moreover, more significant spikes are produced in the output voltage when transitions between $m = \pm 1$ are allowed in a single cell. This is discussed in the following section.

***3) Voltage Spikes and Partition of the Input Domain:*** As it is well known, to avoid short circuits of the cell capacitors, a dead time $T_d$, which delays the turn-ON pulses, must be included in the gate signals. The effect of the dead time on each cell

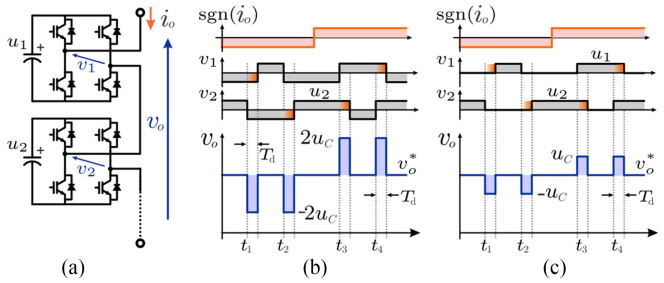


Fig. 3. (a) Dead-time effect during complementary switch of two cells: (a) Two cells of the cluster; (b) full-domain operation with $m_j \in [-1.1]$; (c) partitioned-domain implementation with $m_j \in [-1, 0]$ or $[0, 1]$.

can be summarized as follows [33]: transitions from $s_x = 1$ to $s_x = -1$ are only affected when the current polarity is positive, $i_o > 0$, since the switching state during $T_d$ is $s_x = 1$ even when the demanded state is $s_x^* = -1$. Conversely, if the transition from $s_x = -1$ to $s_x = 1$ is realised when $i_o < 0$, the switching state during $T_d$ is $s_x = -1$ even when $s_x^* = 1$.

Therefore, during dead-time transitions undesirable voltage spikes in the output voltages of the cells could be produced when two or more cells simultaneously switch between $s_x \pm 1$ [20]. This is illustrated using Fig. 3(a). Let us assume that the demanded cluster voltage $v_o^*$ remains constant but the position of the cells in the priority list has changed. Then, according to the greedy algorithm, the first cell would have to switch from $s_1 = -1$ to $s_1 = 1$ and the second one in the opposite direction, i.e., from $s_2 = 1$ to $s_2 = -1$ to maintain the same output voltage, as shown in Fig. 3(b) at instant $t_1$. However, due to the dead-time influence, the first cell remains in the state $s_1 = -1$ during $T_d$ producing an output voltage error of approximately $-2u_C$, where $u_C$ is the average voltage of the cells being switched. Additionally, during the transition after instant $t_3$, the output voltage error is $2u_c$ because the second cell does not switch immediately from $s_2 = 1$ to $s_2 = -1$. The other two combinations where undesired spikes of amplitude $2u_C$ are produced are shown at instants $t_2$ and $t_4$.

Nevertheless, the amplitude of the voltage spikes can be halved when transitions are limited from $s_x = 0$ to $s_x = \pm 1$ and vice versa, as shown in Fig. 3(c). Therefore, the original domain in (3c) is divided into two subsets, i.e., $m_j \in [0, 1]$ and $m_j \in [-1, 0]$. Thereby, depending on the voltage reference polarity, the greedy algorithm is performed over one of these subsets always starting with all cells bypassed, i.e., $m = 0$.

An explicit description of this procedure for $v_o^* > 0$ is shown in Algorithm 1, where a running time of $O(n)$ is achieved. Because only one cell per period is modulated and the rest of cells either are in the ON state or bypassed, this solution approach is suitable for applications based on LS-PWM.

***4) Extended Formulation for NLM:*** The previous algorithm can be easily extended to the NLM strategy by simply restricting the domain of the modulation indexes to $m_j \in \{-1, 0, 1\}$. Under this perspective, the only modification

**Algorithm 1:** Greedy Algorithm for $v_o^* > 0$.

**Inputs:** $v_o^*$, $i_o$, $\mathcal{N}$, and $\mathcal{U}$;
**if** $i_o > 0$ **then** ▷ charging state
  **for** $j = 1$ to $n$ **do**
    $\mathcal{N}_j = \mathcal{N}_{n-j+1}$; ▷ sorting in increasing order
$m :=$ zeros$(n)$; ▷ all cells are assigned with $m = 0$
$u_\Sigma := 0$;
**for** $j = 1$ to $n$ **do**
  $\ell := \mathcal{N}_j$;
  **if** $u_\Sigma + u_{C\ell} \leq v_o^*$ **then**
    $m_\ell := 1$;
    $u_\Sigma := u_\Sigma + u_{C\ell}$;
  **else**
    $m_\ell := \frac{1}{u_{C\ell}}(v_o^* - u_\Sigma)$; ▷ for the cell to be modulated
    **break**;
**Output:** $m$;

to the Algorithm 1 must be realised in the $\ell$th iteration, when the first overshoot respect to the voltage reference is produced. Thus, the $\ell$th modulation index can be computed as follows:

$$m_\ell = \text{round}\left(\frac{1}{u_{C\ell}}\left(v_o^* - \sum_{j=1}^{\ell-1} u_{Cj}\right)\right) \tag{13}$$

with round$(\cdot)$, a function that rounds its argument to the nearest integer. Therefore, the computational burden of the NLM method is very similar to that required to solve (**P2p**).

## III. Conditions and Control System for Testing the CVB Strategies

To analyze the performance of modulation algorithms, typically some performance criteria, e.g., harmonic distortion versus modulation index, are utilized. However, for MMCs, these goodness factors cannot be directly applied since the modules are composed of floating capacitors and a current flow in the cluster is required to balance them [4], [6]. Besides, depending on the load operation point, oscillations of different amplitude and frequency are produced in the capacitor voltages. To make a fair comparison of all the CVB methods evaluated in this paper, it is necessary to operate the MMC in the same operating point, including identical voltage ripple in the capacitors.

Assuming that each instantaneous capacitor voltage is close to the desired value $U_C^*$, the following small signal model for the capacitor voltage ripple $\Delta u_C$ can be derived [17]:

$$nCU_C^* \frac{\mathrm{d}\Delta u_C}{\mathrm{d}t} = p_o - p_{\text{loss}} \tag{14}$$

where $p_o$ and $p_{\text{loss}}$ are the instantaneous power and the total losses of the cluster, respectively.

Under steady-state operation, the voltage between the terminals of a branch (see Fig. 4) can be assumed as $v_s = V_s \cos \omega_s t$, and both the current and the fundamental cluster voltage

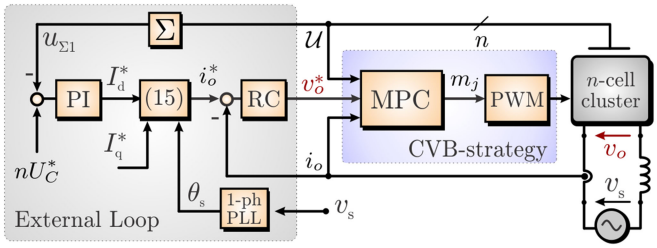


Fig. 4. General control scheme for testing the CVB strategies.

can be decomposed respectively in two orthogonal terms as follows:

$$i_o = I_d \cos\omega_s t - I_q \sin\omega_s t\,,\ v_o = V_{od} \cos\omega_s t - V_{oq} \sin\omega_s t. \tag{15}$$

Hence, the instantaneous power of the cluster is

$$p_o = \tfrac{1}{2}(V_{od} I_d + V_{oq} I_q) + \tfrac{1}{2} V_o I_o \cos(2\omega_s t + \theta_v + \theta_i) \tag{16}$$

where $V_o$ and $I_o$ are the amplitudes, and $\theta_v$ and $\theta_i$ are the phase angles of $v_o$ and $i_o$, respectively.

Typically, the capacitors operate with a fixed average voltage reference, thus, according to (14), the first term on the right hand of (16) must be approximatively zero since the converter losses are very low. Therefore, only the oscillating power in (16) will produce a sinusoidal voltage ripple whose amplitude is approximately given by

$$|\Delta u_C| \approx \frac{(V_s - \omega_s L_B I_q) I_q}{4\omega_s C n U_C^*} = \frac{m_0 I_q}{4\omega_s C}. \tag{17}$$

In consequence, to keep constant the magnitude of $\Delta u_C$ against changes in the modulation index $m_0$, it is required to regulate both $V_s$ and $I_q$ in order to satisfy (17).

Fig. 4 shows the overall control system for testing the CVB strategies analyzed in this paper. The inputs to the MPC-block are the capacitor voltages, the cluster current, and the output voltage to be modulated $v_o^*$, whereas the output is the modulation index $m_j$ of each cell. On the other hand, the external control loop is based on a nested structure where the outer PI controller allows regulating the total energy available in the cluster. The inner current loop is based on a resonant controller (RC), whose reference signal is obtained from (15) by using a single-phase PLL [34].

Notice that in the system of Fig. 4, the proposed CVB methods are tested considering an inductance at the output, which consumes reactive power only. However, this is not really important considering that the converter itself is always consuming reactive power in the steady-state operation regardless of the power factor at the load. This is a well-known issue as reported in several papers where control systems for different topologies of MMCs are discussed (see [6], [8], and [35]).

## IV. Experimental Results

This section presents the experimental results for the proposed CVB strategies considering a nine-cell cluster configuration. The laboratory setup with the details of the experimental parameters is depicted in Fig. 5.

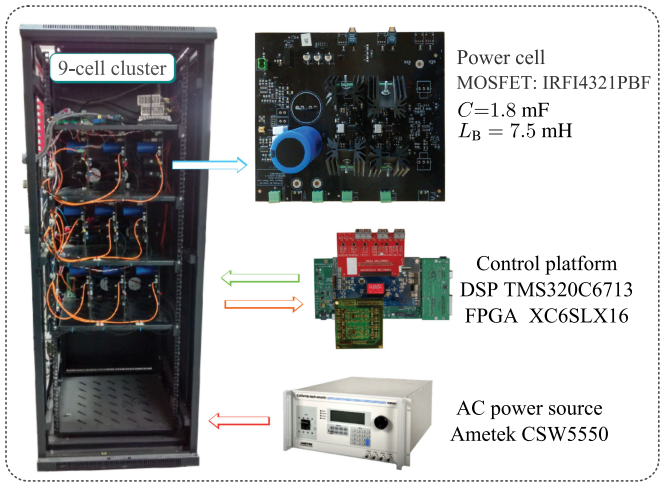


Fig. 5. Downscaled experimental prototype of nine-cell full-bridge cluster.

The control algorithms were implemented in a DSP board based on the Texas Instrument DSK6713 platform augmented with a Xilinx FPGA Spartan 6 based board, as shown Fig. 5. Optical fiber links are used to transmit the switching signals to the IGBT gate drivers. The FPGA platform is programmed to handle the analog-to-digital converters as well as to implement the PWM algorithms. The OSN depicted in Fig. 2(c) are also programmed in this Xilinx FPGA.

To experimentally compare the performance of all the CVB methods fairly, the inner current loop based on RCs (see the control scheme illustrated in Fig 4) is designed with the same bandwidth for all the CVB strategy implemented in this section. Additionally, since two multicarrier PWM schemes are used, it is desired that both the switching frequency ($f_{sw}$ = 450 Hz) and the equivalent switching frequency of the output waveform ($f_o$ = 8.1 kHz) be equal for all CVB schemes. In consequence, the carrier frequency is set to 0.45 and 8.1 kHz for PS- and LS-PWM, respectively.

Experimental results include both steady-state and dynamic operating conditions. The performance of the proposed strategies are compared with that obtained with two well-known CVB methods that have been previously discussed in the literature (see Section IV-B).

### A. Proposed CVB Strategies

***1) Method-I, Dual CVB Technique:*** The experimental results obtained using the dual CVB technique are depicted in Fig. 6, considering three different modulation indexes ($m = 0.4$, $m = 0.6$, and $m = 0.9$). Because of the reduced number of channels available in the digital scope, only three of the nine capacitor voltage waveforms are shown. The average values are depicted at the right-hand side of the scope shots and, as shown in Fig. 6, the capacitor voltages are well regulated (≈33.3 V)

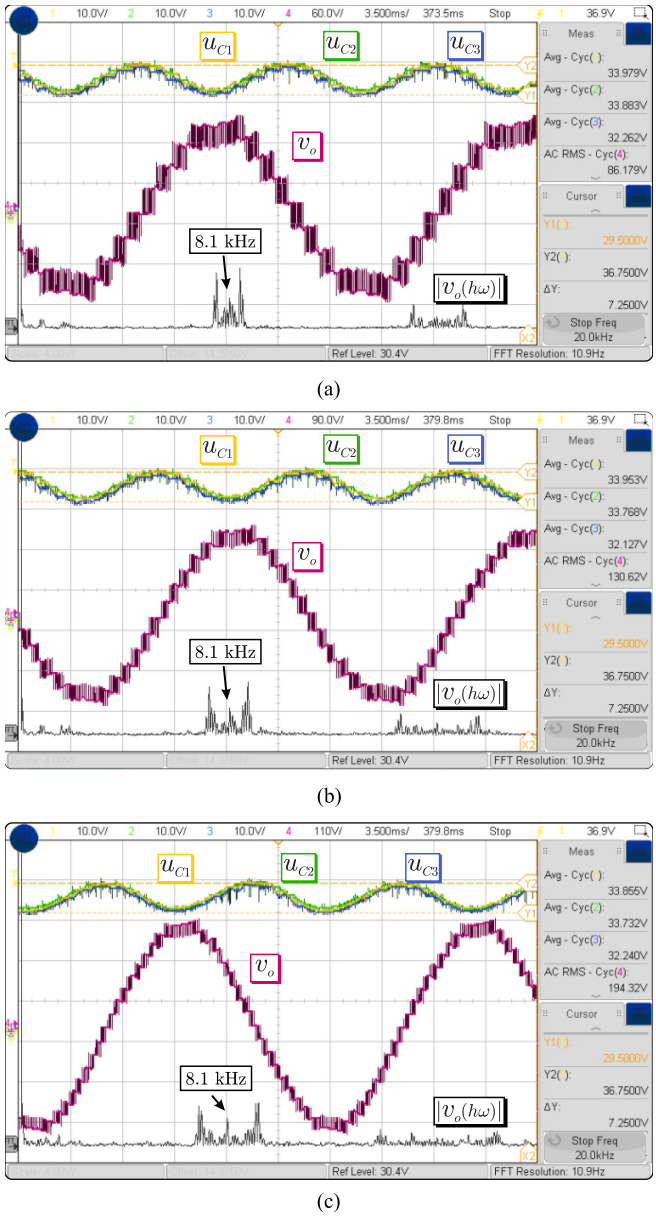


Fig. 6. Method-I: Experimental waveforms for nine cells with 1000 var: (a) $m = 0.4$ with $v_o$[60 V/div]; (b) $m = 0.6$ with $v_o$[90 V/div]; and (c) $m = 0.9$ with $v_o$[110 V/div]. For all cases $|v_o(h\omega)|$ [4 V/div] and $u_{Cj}$[10 V/div].

with a ripple of ≈7.25 V for all the cases. This experimentally validates the methodology presented in Section III to keep constant the magnitude of the capacitor voltage ripple even when the modulation index is changed.

Experimental results considering $m = 0.9$ are shown in Fig. 6(c). From this graphic it is concluded that 19 levels are generated in the output voltage (the maximum available for this number of cells), which are reduced to nine when the modulation index is changed to $m = 0.4$ [see Fig. 6(a)]. This behavior is typical of a PS-PWM strategy.

The cluster voltage frequency spectrum is obtained using the FFT feature embedded in the digital scope firmware (considering 2 kHz/division). As shown in Fig. 6, the first dominant high-frequency harmonics are centered around 8.1 kHz for all the cases, which is consistent with the number of cells and the set carrier frequency (450 Hz) utilized in this experiment. However, the frequency components at 0.9 and 1.8 kHz are not completely cancelled mainly because not all the cells are operating with exactly the same modulation index at a given sampling time [see (7)].

***2) Method-II, Primal CVB Technique:*** The experimental results obtained using this CBV technique are shown in Fig. 7 considering two modulation indexes ($m = 0.6$ and $m = 0.9$). Fig. 7(a) and (b) shows the performance obtained utilizing the greedy algorithm with the original domain $m_j \in [-1, 1]$. Fig. 7(c) and (d) shows the same operating conditions but using the partitioned-domain implementation (see Section II.B), i.e., $m_j \in [0, 1]$ for $v_o^* > 0$ and, $m_j \in [-1, 0]$ for $v_o^* < 0$.

Focusing on the output voltage (purple waveforms), it is concluded that both methods produce output voltage spikes, but they clearly have a larger magnitude when the first approach is used, where each cell $m_j$ could change in the range $m_j \in [-1, 1]$ in a single sampling time. On the other hand, for both implementations, the capacitor average voltages are close to their reference value (33.3 V). However, the first approach [see Fig. 7(a) and (b)] produces a larger capacitor voltage ripple since the modules are continuously switching between $m = \pm 1$. This certainly produces a higher ac ripple in the capacitor currents. Taking all these issues into consideration and unless otherwise stated, in the rest of this paper Method-II is implemented using Algorithm 1.

Regarding the harmonic spectrum of the output voltage [see $|v_o(h\omega)|$ in Fig. 7(c) and (d)], the dominant high-frequency harmonics appear around the carrier frequency $f_c = 8.1$ kHz. The shape of the spectrum is coincident with the typical LS-PWM harmonic spectrum, where the dominant harmonics correspond to the carrier frequency.

## B. Performance Comparison With Other CVB Strategies

The proposed CVB strategies are compared with two well-known CVB strategies, which have been reported in the literature: The first one only uses the minimum and maximum capacitor voltage values in the cluster [21], [22]. Because of its similarity with the primal CVB technique, it is denoted as Method-II(b) or min/max in the rest of this paper. The second strategy uses additional control loops based on PCs to locally compensate each cell [18], [19]. To allow a fair comparison, a slight modification to this strategy is implemented in this paper to cancel the total output voltage error produced by the signals added locally by the CVB loops. The resulting signal flow of the modified local balancing strategy is illustrated in Fig. 8. This method is denoted as Method-III.

For comparison purposes, the following performance indexes are considered: capacitor voltage error, output voltage error, and harmonic distortion of the cluster voltage.

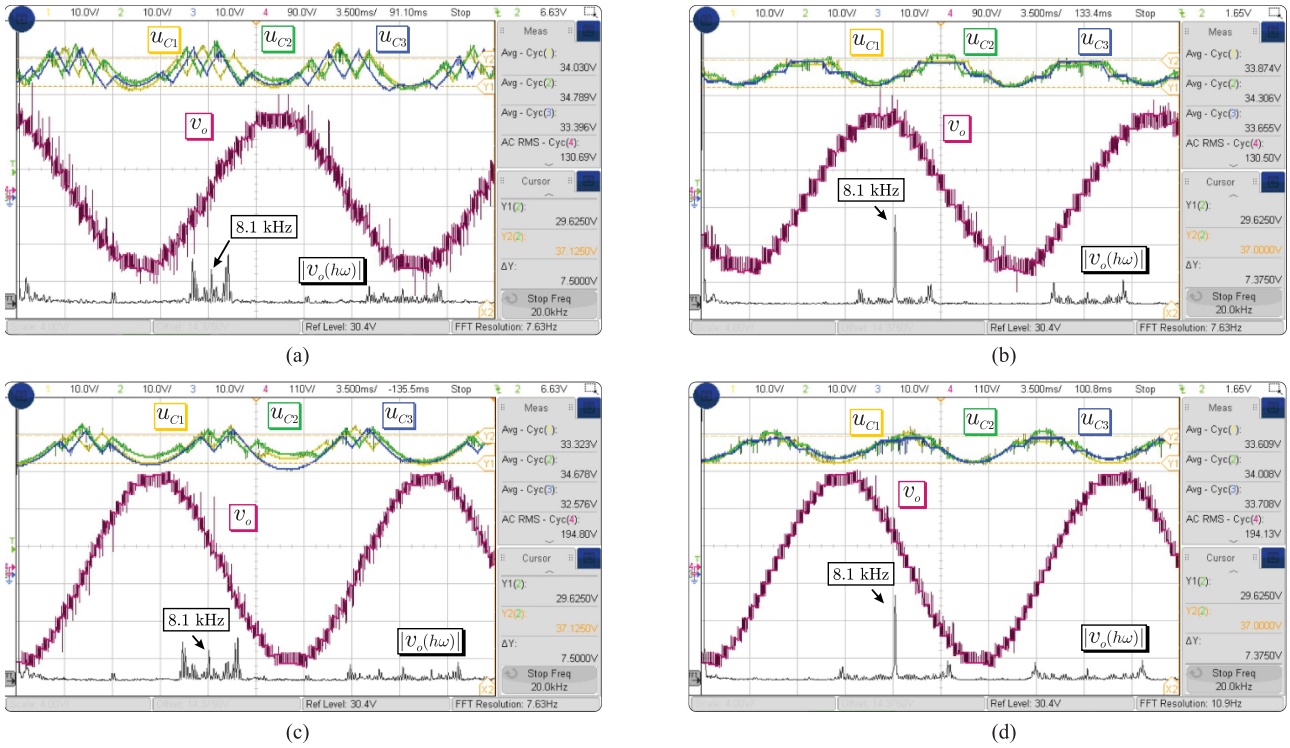


Fig. 7. Method-II: Experimental waveforms for nine cells considering 1000 var with $m = 0.6$ and $m = 0.9$, respectively: (a) and (b) Greedy algorithm with $m_j \in [-1.1]$. (c) and (d) Greedy algorithm with two subsets $m_j \in [0, 1]$ or $m_j \in [-1, 0]$ depending on the sgn$\{v_o^*\}$. Scale: $v_o$[90 V/div] for $m = 0.6$, and $v_o$[110V/div] for $m = 0.9$, $|v_o(h\omega)|$ [4 V/div], and $u_{Cj}$[10 V/div].

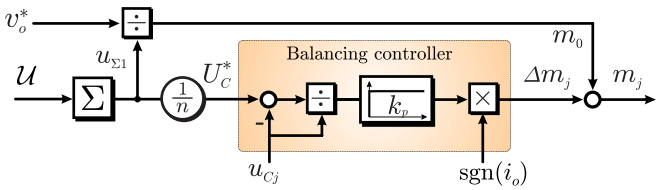


Fig. 8. Signal flow of the Method-III.

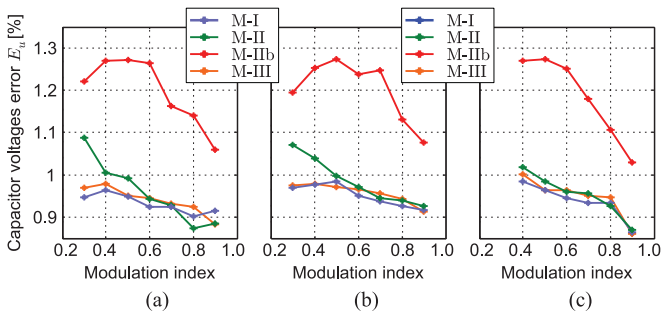


Fig. 9. Comparison of $E_u$: (a) 500 var; (b) 1000 var; and (c) 1500 var.

For all the results presented in this section, the comparison is realised considering operation along the linear modulation range for three different levels of reactive power in the cluster: 500, 1000, and 1500 var. The modulation ranges are selected considering the thermal limits of the converter. Hence, the modulation indexes selected are $m_o \in [0.2 - 0.9]$ for 500 var, $m_o \in [0.3 - 0.9]$ for 1000 var, and $m_o \in [0.4 - 0.9]$ for 1500 var. The ripple of the capacitor voltages is regulated to a constant value by modifying the peak values of $v_s$ and $I_q^*$ according to (17). The dc-reference value for the capacitor voltage is $U_C^* = 33.3$ V and the fundamental frequency utilized is 50 Hz. In addition, the computational burden of each CVB strategy is represented by their DSP processing time.

***1) Capacitor Voltages Error:*** The first performance index to be considered is obtained using (18) and it is representative of the cost value obtained for each CVB compared in this paper:

$$E_u = \frac{1}{N_p} \sum_{k \in \mathcal{S}} \frac{1}{nU_C^*} \sqrt{\sum_{j \in \mathcal{C}} \left(U_C^* - u_{Cj}[k]\right)^2} \tag{18}$$

where $N_p = T_o/T_s$ is the number of samples per fundamental cycle, and $\mathcal{S} = \{1, \ldots, N_p\}$.

The values of $E_u$ obtained experimentally are summarized in Fig. 9. As aforementioned, three reactive power levels are considered for operation along the linear modulation range. As depicted in Fig. 9, Method-I (blue line) produces a better performance than Method-II (green line). In this comparison, the CVB strategy based on the min/max elements of the capacitor voltages (red line) has the worst behavior.

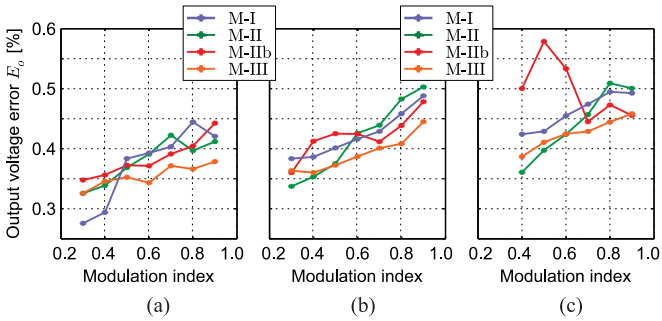


Fig. 10. Comparison of $E_o$: (a) 500 var; (b) 1000 var; and (c) 1500 var.

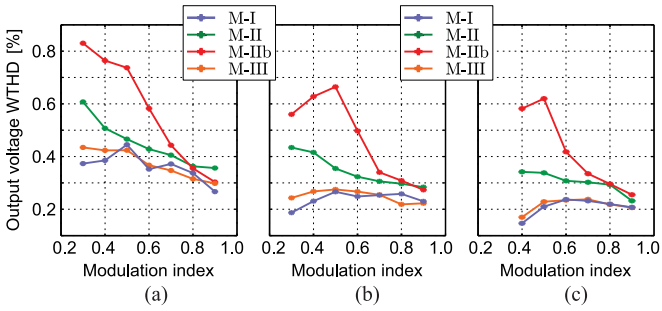


Fig. 11. WTHD comparison: (a) 500 var; (b) 1000 var; and (c) 1500 var.

TABLE I
MEASURED EXECUTING TIME FOR ALL CVB METHODS

| Method | I | II | III |
|---|---|---|---|
| Processing time [$\mu$s] | 15.9 | 1.86-3.92 | 13.2 |

***2) Output Voltage Error:*** To measure the accuracy of the balancing methods respect to the constraint (1c), the error between the output voltage $v_o$ (averaged over each switching cycle) and the reference $v_o^*$ (provided at the current controller output) is considered as the second comparison criterion. The corresponding output voltage error is computed as follows:

$$E_o = \frac{1}{U_C^*}\sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{S}}\left(v_o^*[k]-\bar{v}_o[k]\right)^2}. \tag{19}$$

From Fig. 10, it is concluded that the errors achieved by all CVB strategies are less than 1% of the output and there are no significant differences between them. Then, in practice, all strategies produce a good tracking of the demanded output voltage $v_o^*$ represented by constraint (1c).

Finally, the weighted total harmonic distortion (WTHD) in the voltage $v_o$ is computed for each method and summarized in Fig. 11. From that graphic it is concluded that the CVB methods based on PS-PWM present the best performance. The min/max scheme possess the highest WTHD for all cases.

***3) Algorithm Executing Times:*** The overall executing time for all methods are summarized in Table I. The methods based on the greedy algorithm have the lowest executing times. This good result is partially explained because of implementation issues. For methods M-I and M-III, the algorithms were completely programmed in the DSP and, on the other side, for methods M-II and M-IIb, the greedy algorithm was implemented in the DSP while the OSN was directly programmed in the FPGA. This leads to a reduced computational burden.

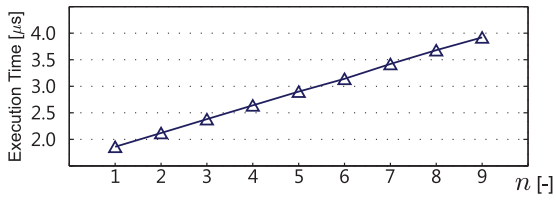


Fig. 12. Processing time of the greedy algorithm.

Additionally, for M-II and M-IIb, the execution time is variable because the greedy algorithm stops when the first overshoot respect to the voltage reference is produced. Therefore, its executing time depends on the number of cells required to modulate $v_o^*$. Fig. 12 shows the executing time of the greedy algorithm versus the output voltage levels in the cluster. This result experimentally validates its theoretical processing time $O(n)$. Furthermore, from Fig. 12, it is concluded that the additional execution time per cell added into the greedy algorithm was $\approx$0.26 $\mu$ s, value which can be useful to estimate the maximum number of modules for which this algorithm is suitable. For instance, if the time to perform the greedy algorithm is limited to half the sampling period, the maximum number of cells for which this algorithm could be implemented is $n_{\max} = 230$ modules (considering the same digital control platform) for a sampling frequency of 8.1 kHz. Notice that this figure is based mainly in the processing time of the greedy algorithm and other time delays, as for instance those produced by the handling and conversion time of the ADCs, have not been considered. However, from this analysis it is fair to conclude that the application of the greedy algorithm to MMC-CVB is a very efficient methodology.

## C. OFF–ON Test

This test consists on temporarily disabling the balancing control scheme, activating it again when any of the cell capacitor voltages reaches a threshold of $\pm 50\%$ of their reference value. The resulting capacitor voltage waveforms for all strategies are shown in Fig. 13. Method-I and II (including min/max approach) show the fastest recovering response, with balancing times around 10 ms and 5 ms, respectively. For this test, Method-III shows the poorest dynamic performance. Moreover, analyzing the deviation of each capacitor voltage with respect to the average value $\Delta u_{Cj}$, it is concluded that Method-I possess the lowest deviation. Finally, it is also concluded that the method based on the full sorted set (Method-II) has a better overall behavior than that based on the min/max scheme. Fig. 14 shows the output voltage and current waveforms corresponding to the OFF–ON test depicted in Fig. 13(a) and (b).

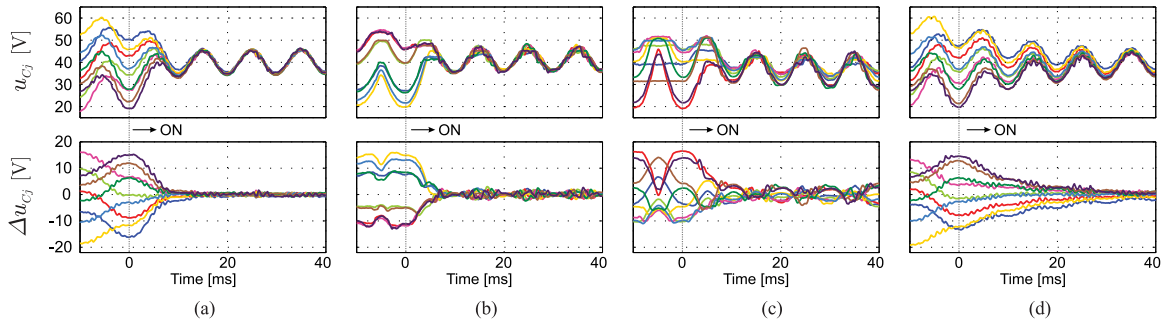


Fig. 13. Capacitor voltage waveforms for OFF–ON testing with $m = 0.7$, $S = 2000$ var, and $nU_C^* = 360$ V: (a) Method-I; (b) Method-II; (c) Method-IIb (min/mix); (d) Method-III. The second row shows the deviation of each capacitor voltage concerning the average value, i.e., $\Delta u_{Cj} = u_{\Sigma 1}/n - u_{Cj}$.

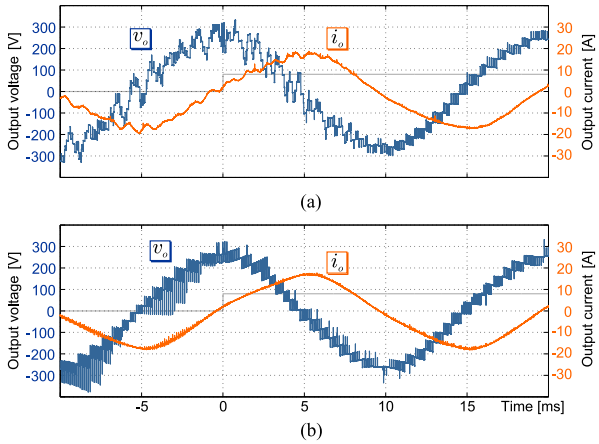


Fig. 14. Output voltage and current waveforms during the OFF–ON test: (a) Method-I; (b) Method-II.

## V. Conclusion

This paper presented two MPC-based CVB strategies. Both methodologies were introduced to efficiently solve the approximated versions of the original control problem, allowing its implementation for the control of converters with a relatively large number of cells per cluster. The first method could be easily integrated with PS-PWM and the second CBV strategy is simple to integrate with LS-PWM. Thus, a cluster voltage with a shaped harmonic spectrum was achieved with both methods.

The experimental results validated the effectiveness of the proposed strategies since both methods achieve the control targets stated in the original optimization problem, i.e., the capacitors are well-balanced, and the synthesized cluster output voltage shows a good tracking of the reference.

The proposed dual CVB method has a steady-state response similar to the existing PS-PWM based CVB algorithm. Nevertheless, its dynamic performance is much faster. On the other hand, the primal CVB method produces a slightly higher harmonic distortion than that produced by the PS-PWM based methods due (mainly) to the voltage spikes. However, the experimental results showed that this strategy presents the fastest dynamic performance.

The computational burden of the dual CVB strategy was slightly higher than the existing PS-PWM based CVB algorithm. On the other hand, the use of the greedy algorithm with an OSN allowed the primal CVB strategy scalability to be applied in MMCs with a large number of cells.

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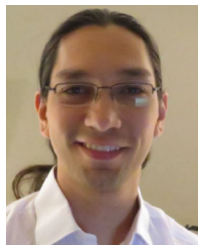

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Dr. Lezana was the recipient of the IEEE Transactions on Industrial Electronics Best Paper Award in 2007.