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CASCADED OPTIMAL SWITCHING SEQUENCE MODEL PREDICTIVE CONTROL FOR THE 3L-NPC WITH LC FILTER

TESIS PARA OPTAR AL GRADO DE MAGÍSTER EN CIENCIAS DE LA INGENIERÍA, MENCIÓN ELÉCTRICA

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CONTROL PREDICTIVO BASADO EN MODELOS CON SECUENCIA DE CONMUTACIÓN ÓPTIMA PARA EL 3L-NPC CON FILTRO LC

En este trabajo, una estrategia de control predictivo basado en secuencia de conmutación óptima es propuesta para el control de voltaje de un convertidor de tres niveles con enclavamiento al punto neutro (3L-NPC) con filtro LC conectado en sus terminales de salida. La estrategia es una extensión del método denominado control predictivo con secuencia de conmutación optima propuesto en la literatura para el control de corriente y potencia del 3L-NPC conectado a la red.

La estrategia resuelve dos problemas de optimización en cascada. El primer problema encuentra la secuencia optima de vectores de conmutación del convertidor y sus correspondientes ciclos de trabajo que asegure un seguimiento de las variables de salida del sistema. Mientras, el segundo problema utiliza la solución encontrada por el primero para calcular una señal de secuencia cero óptima para balancear la tensión en los capacitores del enlace DC.

Resultados en simulación y experimentales demuestran que la estrategia logra exitosamente controlar la tensión de salida y la corriente del convertidor mientras mantiene balanceada la tensión en el punto neutro de los capacitores del enlace DC.

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CASCADED OPTIMAL SWITCHING SEQUENCE MODEL PREDICTIVE CONTROL FOR THE 3L-NPC WITH LC FILTER

In this thesis, an Optimal Switching Sequence MPC (OSS-MPC) algorithm is proposed for the three-level neutral-point-clamped (3L-NPC) inverter with output LC filter. The strategy is an extension of the Cascaded Optimal Switching Sequence MPC (C-OSS-MPC) proposed in the literature for current and direct power control of active front-end 3L-NPC inverters.

The strategy solves two cascaded optimization problems. The first problem finds the sequence of optimal switching vectors and their corresponding duty cycles to track the output variables of the converter. Then, the second optimization problem use the solution provided by the first to find an optimal zero sequence injection signal to balance the voltage in the DC-link capacitors.

Extensive simulation and experimental results show that the control strategy successfully controls the load output voltage and the converter current while keeping balanced the voltage in the capacitors of the DC-link.

Dedicada a la memoria de aquellos que partieron
Mis abuelos, José Ibáñez y Oscar Herrera;
Mi abuela, María Espinosa;
Y mi padrino, Juan Carlos Encina.

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Contents

List of Tables

List of Figures

Chapter 1

Introduction

Energy has shaped our civilization. Up to this point in time, humanity has learned to exploit more and more sources of energy [1]. From our own physical strength improved through sticks and stones as tools and weapons, to fire and fuel. Each mastered source brought new technological advances, new forms of social organization, and new individual skills to master. Today, we enjoy the comfort brought by industrialization and the technologies powered by the underground treasures: coal, gas and oil. However, our extended and heavy consumption of these fuel sources is destroying the planet.

Global warming is defined as the increase in the surface average temperature of the earth due to the increased concentration of greenhouse gases (GHGs) [2]. Greenhouse gases -such as water vapor, carbon dioxide, methane, ozone, and nitrous oxide- in adequate amounts make life on earth possible. However, burning fossil fuels to produce energy has increased their concentration in the atmosphere [3]. This has dire consequences for life on earth such as: temperature rise, change in chemistry and temperature of oceans, increased ocean levels, death of plants and animals, etc. If humanity wants a future on earth, it needs to adapt to climate change. For that, we need to reduce our dependency on fossil fuels replacing them with new energy sources.

Renewable energy, along with other technologies, are the main strategy to reduce carbon dioxide emissions in critical industry sectors by 2050 [4]. The most used renewable energy sources are wind and solar [5]. Energy is harvested from these sources through wind turbines and solar photovoltaic panels interfaced to the grid through power electronics converters. This sources are intermittent in nature; thus, electricity storage technologies are used to backup its operation (e.g. batteries, flywheel, superconductive energy storage, ultracapacitor and pumped hydro) [6]. This storage technology is heavily dependent on power electronics as well.

Power electronics is an area of electrical engineering which studies the control and conversion of electrical energy using electronics circuits [7]. These electronics circuits - called power converters- control the flow of electrical energy from source to load [8]. The converter is a complex system built with semiconductor devices and energy storage components. In Fig. 1.1, the block diagram of a typical power electronics system is shown. The power processor is the interface between source and load. The system variables are measured and send to a controller. The controller decide which semiconductor device will open or close to achieve its objective.

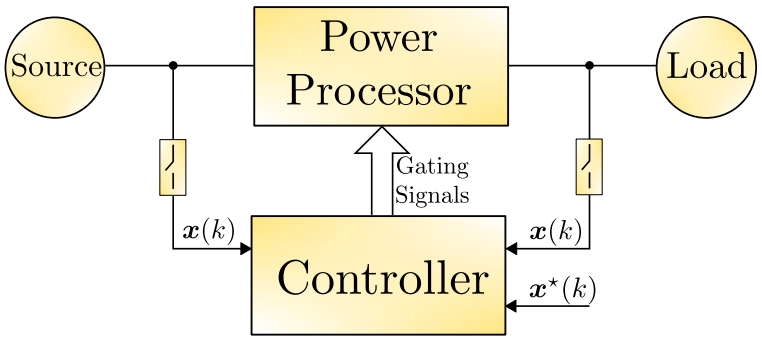


Figure 1.1: Block diagram of a power electronics system.

Semiconductor devices are used as an electronic switch in one of two modes: saturation or blocking [9]. Ideally, this switch should not have a voltage drop when is *on* nor allow current to flow through it when is *off*. Also, it can change state instantaneously. In other words, the ideal switch does not dissipate power when switching nor conducting and neither does the power converter built with them. However, the ideal switch does not exist in reality.

Power electronics converters can be classified according to the waveforms at its input and output terminals. AC/AC converters transform AC waveforms with fixed amplitude and frequency into AC waveforms of variable amplitude and frequency. DC/DC converters take an uncontrolled DC waveform and produce a controlled DC output waveform. DC/AC converters take a DC waveform and transform it into an AC waveform of variable amplitude and frequency. DC/AC converters can operate in two modes: inversion and rectification. Inversion is the process of transforming DC into AC waveform. On the contrary, rectification is the process of transforming an AC waveform into DC. A summary of power conversion is shown in Fig. 1.2.

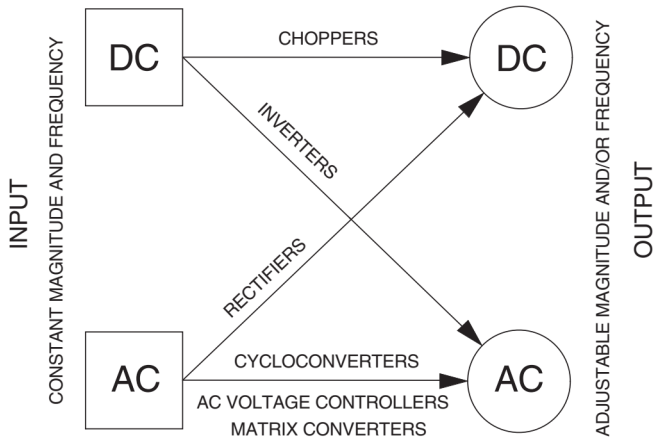


Figure 1.2: Types of electric power conversion and the corresponding power electronic converters (taken from [7]).

The adequate operation of power converters requires the design and implementation of advanced control strategies. Typically, control schemes for power converters are based on linear control techniques with reference frame transformation [10]. When the controlled variables are in the synchronous reference frame, proportional-integral (PI) control is used. However, if the controlled variables are in the stationary reference frame, proportional-resonant (PR)

control should be use to ensure zero error in steady-state operation [11]. In Fig. 1.3, the block diagram of a PI-control scheme in the synchronous reference frame for a current-controlled inverter is shown.

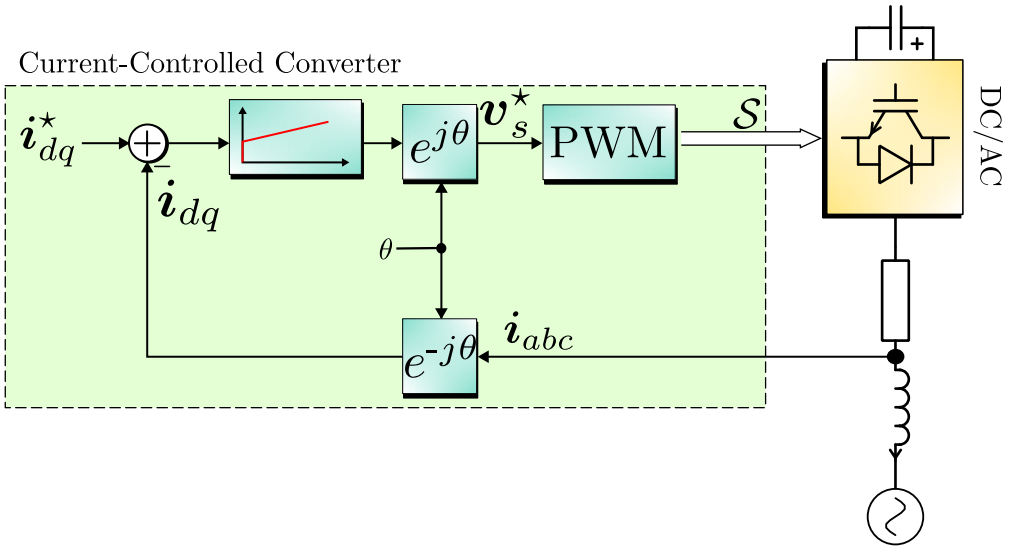


Figure 1.3: Block diagram of a current-controlled PWM inverter in the synchronous reference frame.

When high-quality output voltage is required, an LC filter is connected at the output terminals of the converter [12]. These systems can be found in applications such as uninterruptible power supplies (UPS) [13, 14, 15, 16], energy storage [17], motor drives [18, 19], microgrids [20], and distributed generation [21]. Control of power converters with LC filters typically involves two cascaded PI or PR control loops: an outer voltage control loop, and an inner current control loop [12]. The voltage loop computes the reference for the inner current loop, and the current loop computes the desired converter voltage to be synthesized by a modulation scheme. Other control strategies proposed for voltage control of power converters are deadbeat control [22, 23], feedback linearization control [13], repetitive control [21], hysteresis control [19], sliding mode control [24], adaptive backstepping control [25], iterative learning control [14], and model predictive control [20, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36].

Model Predictive Control (MPC) has been gaining increasing attention in power electronics converters applications [37]. Most common applications include grid-connected converters, inverters with RL load, inverters with output LC filter, and high-performance drives [38, 39, 40]. MPC has several advantages such as easy inclusion of nonlinearities, simple treatment of constraints, the multivariable case can be easily considered, dead times can be compensated, etc [41]. On the other hand, the disadvantage of MPC is his high computational load. However, the exponential development in processing power of microprocessors (such as digital signal processors and field-programmable gate-arrays) has allowed the implementation of MPC algorithms in real-time platforms [42].

A wide variety of MPC algorithm for power electronics converters exist. In Fig. 1.4, a general block diagram for a predictive control algorithm is shown. An MPC algorithm can be considered, in general terms, as any algorithm that uses a model of the system to predict its future behaviour and select the most appropriate control action based on the solution to an optimability criterion [43]. The optimability criterion is evaluated in a cost function and can be, for example, tracking of the system state variables, minimize common-mode voltage, or

reduce the converter switching frequency [37, 43]. After the optimability criterion has been reached, and consequently the best possible solution to the optimization problem has been found, the algorithm sends it to the converter to be synthesized.

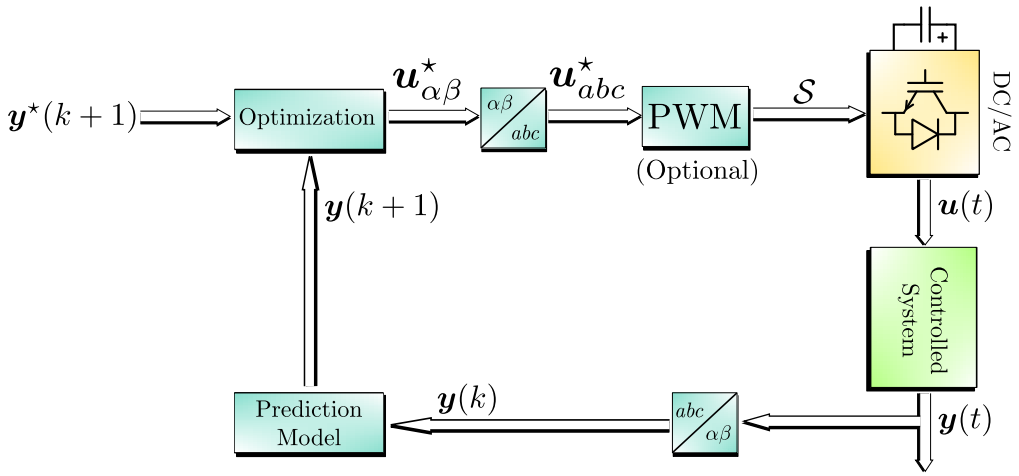


Figure 1.4: Block diagram of an MPC algorithm for power electronics.

MPC algorithms are classified according to the nature of the optimization variable in the control problem. In Fig. 1.5, a classification of predictive control algorithms for power electronics is shown. This classification is reproduced from [37] with some elements of the classification given by [44]. In broad terms, these algorithms for power electronics are classified as Direct MPC or Indirect MPC methods. In direct MPC methods the optimization variable is an integer-valued vector representing the state of the converter switching devices [16]. On the other hand, in indirect MPC the optimization variable is a real-valued vector representing the fundamental component of the converter output voltage [45, 46].

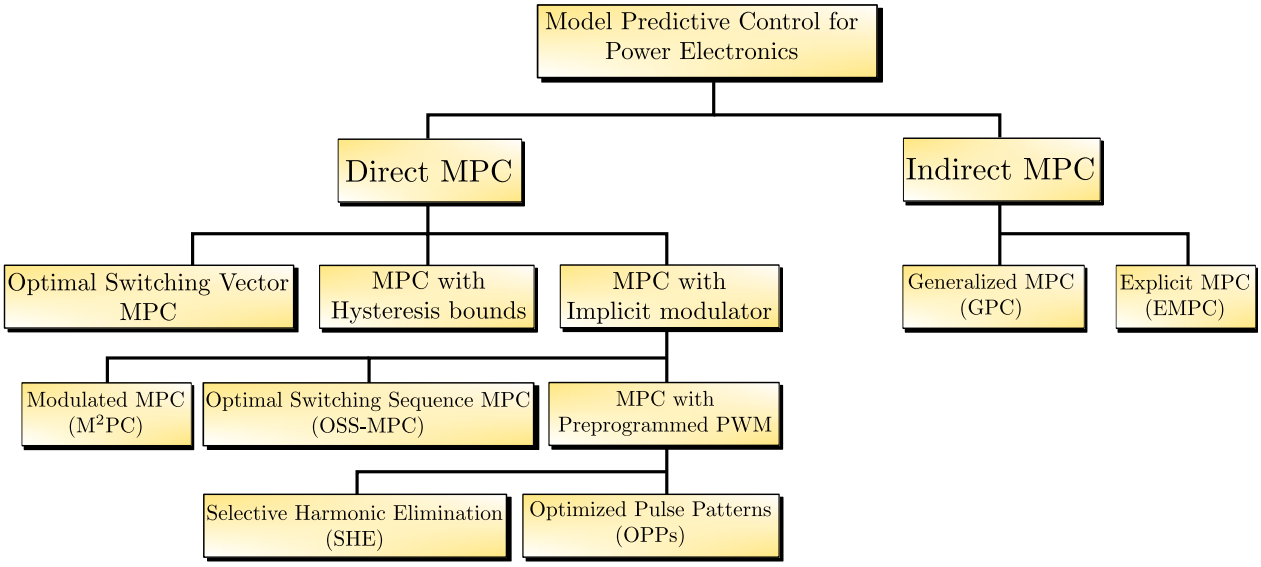


Figure 1.5: Classification of MPC algorithms for power electronics converters.

Direct MPC methods are subdivided into three categories: optimal switching vector MPC

(OSV-MPC), MPC with hysteresis bounds, and MPC with an implicit modulator. OSV-MPC, commonly found as Finite Control Set MPC (FCS-MPC) in the literature, was first proposed to control the output current of a two-level inverter connected to an RL load [47]. Since then, it has been applied to many converter topologies [38]. In this strategy, the converter switches are directly computed and sent to the converter. Thus, allowing direct manipulation of the controlled variables. The advantages of OSV-MPC are an intuitive design procedure, straightforward implementation and fast transient response [37]. However, they come at the cost of pronounced computational complexity and variable switching frequency due to the absence of a modulator [48].

Direct MPC methods with implicit modulator has been proposed to overcome the issue of variable switching frequency introduced by OSV-MPC while mantaining its advantages [49, 50]. These strategies attempt to emulate the behavior of pulse-width modulation techniques. In particular, Optimal Switching Sequence MPC (OSS-MPC) and Modulated MPC (M^2PC) introduce the concept of variable switching time instants [37]. According to the concept of variable switching time instants, the position of the converter switches can change at any moment during a sampling interval. Then, the strategies compute a sequence of switch positions and their corresponding duty cycles to be applied during the next sampling interval. Thus, a fixed switching frequency is achieved resulting in a reduction of harmonic distortion [37]. However, M^2PC is prone to suboptimality because the optimization problem is solved in two stages: first stage to find the optimal switch positions and the second stage to compute the duty cycles [51].

OSS-MPC avoid suboptimal solutions computing the optimal sequence of switch positions and their corresponding duty cycles in one stage. The strategy was first introduced for power control of a grid-connected two-level inverter [50]. Then, the strategy was modified to be used in other converter topologies such as three-level neutral-point-clamped (3L-NPC) inverter and vienna rectifier [52, 53, 54, 55]. In [33], OSS-MPC was used for voltage control of an LC-filtered two-level inverter achieving low output voltage ripple and reduced harmonic content compared against other MPC methods (such as OSV-MPC). However, at the best of the author knowledge, OSS-MPC has not been applied for output voltage control of LC-filtered three-level NPC inverters.

In this work, the OSS-MPC presented in [52, 53] is extended to three-level neutral-point-clamped (3L-NPC) inverters with output LC filter in standalone operation. The control strategy was tested in MATLAB-Simulink® with the PLECS® Blockset package. Then, the strategy was implemented in a Texas Instrument (TI) TMS320F28379D MCU in the LaunchXL-F28379D development kit. The power stage (i.e. the converter and the output LC filter) were emulated by PLECS RT Box Hardware-in-the-Loop (HIL) platform.

1.0.1. Motivation

In Direct MPC methods for power electronics converters, OSV-MPC have several advantages such as fast dynamic response, simple inclusion of constraint and nonlinearities in the control problem, and ease of implementation. However, it suffers from a variable switching frequency. An MPC strategy to avoid the problem of variable switching frequency while keeping the advantages of OSV-MPC denominated as M^2PC was introduced. It uses the concept of variable switching time instants to pose an optimization problem whose solution are a sequence of switching vectors and their corresponding duty cycles to be applied in the converter. However, the strategy solves the optimization problem in two separated sta-

ges which produce sub-optimal solutions. Thus, OSS-MPC was proposed in the literature to overcome the drawback of M^{2}PC while keeping its advantages. In OSS-MPC, the sequence of switching vectors and their duty cycles are found as the solution of one optimization problem. As mentioned before, an OSS-MPC scheme has been introduced in the literature for grid-connected 3L-NPC. However, the method has not been applied for voltage control of the 3L-NPC converter with output LC filter in standalone operation.

1.0.2. Thesis hypothesis

The following hypotheses will guide this work:

- OSS-MPC can achieve good reference tracking of the converter current and load voltage for a three-level neutral-point-clamped converter with output LC filter operating in standalone operation.
- OSS-MPC can keep balanced the voltage of the DC-link capacitors in the three-level neutral-point-clamped inverter.
- OSS-MPC allows the converter to operate with a fixed switching frequency.
- OSS-MPC has a fast dynamic response compared to traditional methods.

1.0.3. Thesis objectives

The general objective of this thesis is to design and implement a predictive control strategy with optimal switching sequence for the three-level NPC converters with output LC filter in standalone operation. The specific objectives are as follows:

- Simplify cascaded linear control schemes often used for voltage control of converters with output LC filter in standalone operation.
- Enable operation of the converter at fixed switching frequency.
- Evaluate the behavior of the proposed control strategy through simulations in MATLAB-Simulink® with the PLECS® Blockset package.
- Test steady-state and transient performance of the control strategy.
- Assess controller performance under three scenarios: without load at the output terminals, linear resistive load connected at the output terminals, and nonlinear three-phase load connected at the output terminals.
- Implement the proposed control strategy in a Texas Instrument (TI) TMS320F28379D MCU in the LaunchXL-F28379D development kit.
- Validate the performance of the proposed control algorithms through their implementation on a microcontroller and testing on Hardware-in-the-Loop (HIL) systems.

Chapter 2

Background Theory

In this chapter, the operational principle of the three-level neutral-point-clamped converter (3L-NPC) will be described. First, the topology is introduced and its operation studied. Then, a mathematical model for the output voltage and DC-link neutral-point voltage is presented. Then, two common modulation schemes for the 3L-NPC will be covered: Carrier-Based PWM, and Space Vector Modulation.
Furthermore, a brief description of the general operation principle of model predictive control schemes will be given.

2.1. 3L-NPC

The 3L-NPC was the first multilevel converter topology proposed by the group of Akagi in [56]. It was introduced around 1980 to reduce the pulsating torque and harmonic losses on AC drives; thus, improving the efficiency and reducing the cost of the system. Nowadays, this converter topology is the standard for medium and high-voltage applications [57, 58]. In the mining industry, for example, 3L-NPC converters are used in variable frequency drives (VFD) for long belt-conveyor systems carrying ore (specifically, the belt-conveyor system in the cited publication was carrying copper.) [59].

2.1.1. Converter description

The converter topology consists of three phases (or legs) connected in parallel, each with four active semiconductor devices with freewheeling diodes per phase; see Fig. 2.1. The active semiconductor switches can be either Insulated Gate Bipolar Transistors (IGBTs) or Gate-Commutated Thyristors (GCTs) [60]. Two series-connected diodes (denominated as clamping diodes) connect the node between the upper-side switching devices (whose switching states are represented by the variables u_{1x} and u_{2x}, where $x \in \mathcal{P} = \{a, b, c\}$) and the node between the lower-side switching devices (whose switching states are represented by the variables $\overline{u_{1x}}$ and $\overline{u_{2x}}$). The node between the clamping diodes connects to the floating neutral-point of the DC-link formed by two cascaded DC capacitors. This connection allows the 3L-NPC to generate three-level output voltages at the AC side of the converter.

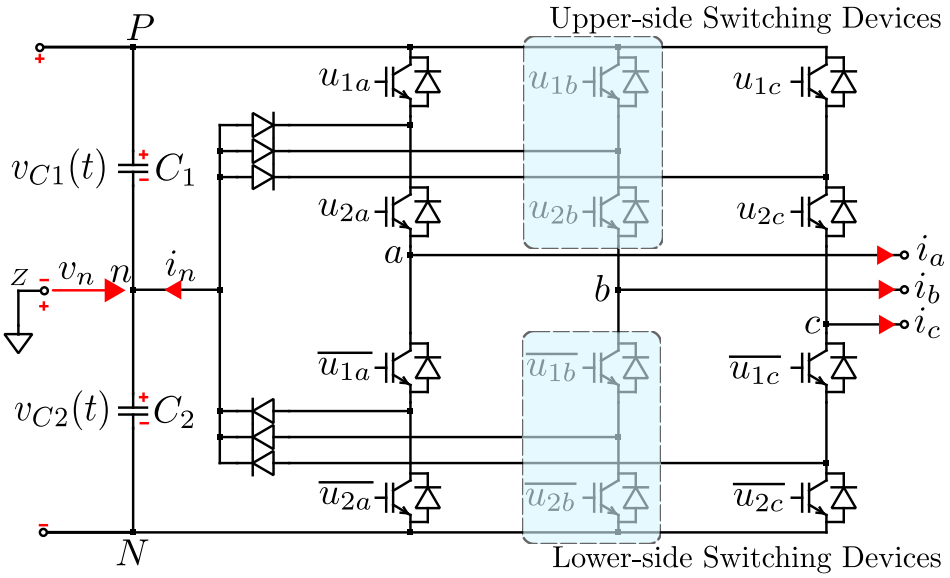


Figure 2.1: 3L-NPC topology.

The turn-on and turn-off of the active semiconductor devices manipulate the electrical variables at both ends of the converter. In this work, we will follow the notation introduced by [61] for the converter variables. The leg switching state summarizes the position of each active device in one of the legs. The discrete variable $u_x \in \{1, 0, -1\}$ represents the switching state for any of the converter legs. Table 2.1 shows the relationship between the phase switching state, the position of the switching devices, and the electrical variables on both sides of the converter.

Table 2.1: Relationship between the switching states per leg and the state of the switching devices.

u_x	u_{1x}	u_{2x}	$\overline{u_{1x}}$	$\overline{u_{2x}}$	i_n	v_x
1	1	1	0	0	0	v_{C1}
0	0	1	1	0	-i_x	v_n
-1	0	0	1	1	0	v_{C2}

The current path through the converter depends on the output current polarity and the leg switching state, as shown in Fig. 2.2. When the upper-side switching devices (u_{1x} and u_{2x}) are *on* and the output current $i_x > 0$, the current flows from the positive rail of the DC-link towards the load through the active devices; as shown in Fig. 2.2(a). In the opposite case, the current flow from the load towards the positive rail of the DC-link through the freewheeling diodes of the upper-side switching devices. The same analysis holds for the two remaining leg switching states, as shown in Fig. 2.2(b) and Fig. 2.2(c).

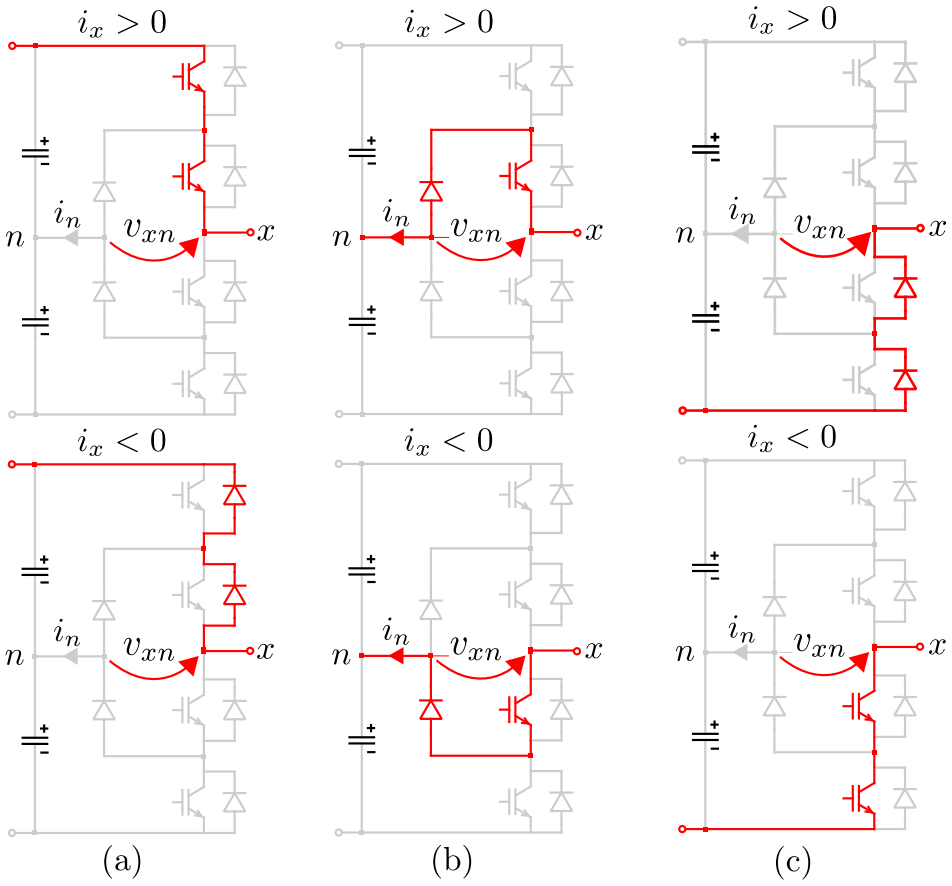


Figure 2.2: Current paths through the 3L-NPC for any leg switching state and output current polarity.

2.1.2. Mathematical model

The switching vector $\boldsymbol{u}_{abc} = [u_a \ u_b \ u_c]^\intercal \in \mathbb{U} \triangleq \{1, 0, -1\}^3$ describes the behavior of all converter legs. The elements of the set $\mathbb{U}$ are 27 triplets that represent all possible switching combinations of the converter. Let's assume that an ideal DC voltage source V_{dc} connects to the DC-link of the converter and that the voltage in each of the DC-link capacitors is equal to half of the DC voltage source (i.e., $v_{C1} = v_{C2} = V_{dc}/2$). The model of the converter output voltage is the following [62]:

$$\boldsymbol{v} = \frac{V_{dc}}{2}\boldsymbol{u}_{abc} + (1 - |\boldsymbol{u}_{abc}|)v_n \tag{2.1}$$

Where $|\boldsymbol{u}_{abc}| = \begin{bmatrix} |u_a| & |u_b| & |u_c| \end{bmatrix}^\intercal$ is the component-wise absolute value of the switching states [61], and v_n is the voltage of the floating neutral point between the DC-link capacitors (see Fig. 2.1).

The switching vector can be mapped to the $\alpha - \beta$ stationary reference frame using the transformation matrix $\boldsymbol{\mathcal{T}}$ defined by eq. (2.2).

$$\boldsymbol{\mathcal{T}} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \tag{2.2}$$

Consequently, the converter output voltage in the stationary reference frame is

$$\boldsymbol{v}_s = \frac{V_{dc}}{2}\boldsymbol{u}_s - \boldsymbol{\mathcal{T}}|\boldsymbol{u}_{abc}|v_n \tag{2.3}$$

The transformation $\boldsymbol{u}_s = \boldsymbol{\mathcal{T}}\boldsymbol{u}_{abc} = \begin{bmatrix} u_{s\alpha} & u_{s\beta} \end{bmatrix}^\intercal \in \mathcal{U} \triangleq \boldsymbol{\mathcal{T}}\mathbb{U}$ generates 19 non-redundant switching vectors and 8 redundant switching vectors in the stationary reference frame, see Fig. 2.7(a). Vectors in the stationary reference frame who are mapped from different vectors in the *abc*-coordinate system are called redundant. For example, vectors $\begin{bmatrix} 1 & 1 & 0 \end{bmatrix}^\intercal$ and $\begin{bmatrix} 0 & 0 & -1 \end{bmatrix}^\intercal$ map to $\begin{bmatrix} 0.5 & 0.866 \end{bmatrix}^\intercal$. Redundancy is an important property which can be taken advantage of to achieve some control objectives, as will be explained in regard to the balance of the neutral-point voltage between the DC-link capacitors.

The main challenge for the proper operation of this converter is to keep the capacitor voltages balanced. The balancing of the capacitor voltages can be visualized through the neutral-point (NP) voltage, defined as $v_n = \frac{1}{2}(v_{C2} - v_{C1})$. It follows that by assuming a constant DC-link voltage and taking into account that $i_a + i_b + i_c = 0$, the NP-voltage dynamic can be modelled as [61, 62]:

$$\frac{\mathrm{d}v_n}{\mathrm{d}t} = k_c i_n \quad ; \quad k_c = \frac{1}{C_1 + C_2} \tag{2.4}$$

with the NP-current given by:

$$i_n = |\boldsymbol{u}_{abc}|^\intercal \boldsymbol{\mathcal{T}}^{-1} \boldsymbol{i}_{\alpha\beta}, \tag{2.5}$$

being $\boldsymbol{i}_{\alpha\beta} = \begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^\intercal$, the three-phase converter current mapped into the $\alpha\beta$ frame.

2.2. Pulse-Width Modulation

The fundamental idea behind power converters is the transformation of electrical energy from one form to another. Inverters, for example, take electrical variables (either voltage or current) in DC form and transform them into AC waveforms. For this, the power converter produces a switched waveform whose average value is equal to some desired reference signal [63]. The desired reference signal is received by a modulator who choose the active semiconductor devices that have to be turned on and off throughout one cycle, see Fig. 2.3(a) and Fig. 2.3(b).

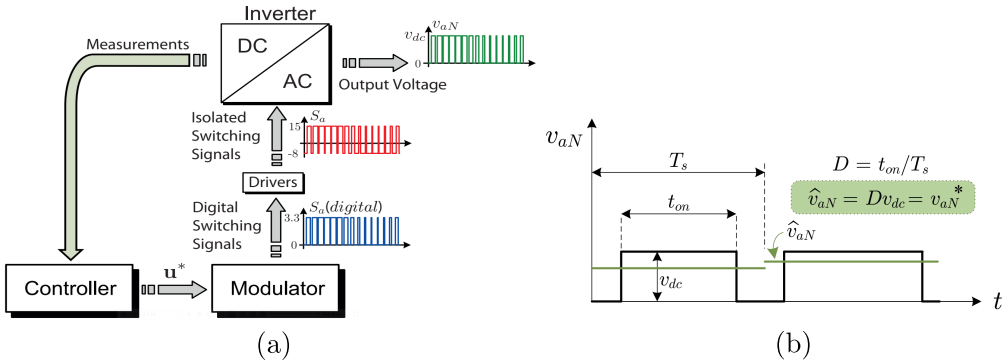


Figure 2.3: General operation scheme for a power converter. (a) Elements of the modulation strategy, and (b) Converter average output voltage (taken from [63]).

In DC-AC Voltage Source Converters (VSCs) the two most used modulation schemes are Carrier-Based PWM (CB-PWM) and Space Vector Modulation (SVM). Both schemes differ in concept and implementation [64]. CB-PWM modulates each phase separatedly comparing the desired voltage waveforms with a high-frequency triangular reference signal, see Fig. 2.4(a). It can be implemented using analog circuits. On the other hand, SVM treat the converter as one discrete unit depicted with the switching vectors, see Fig. 2.4(b). It needs digital processors to perform the computations of the modulation algorithm. In spite of their differences, it has been proved that both strategies are equivalent in harmonic performance and DC-link utilization [63].

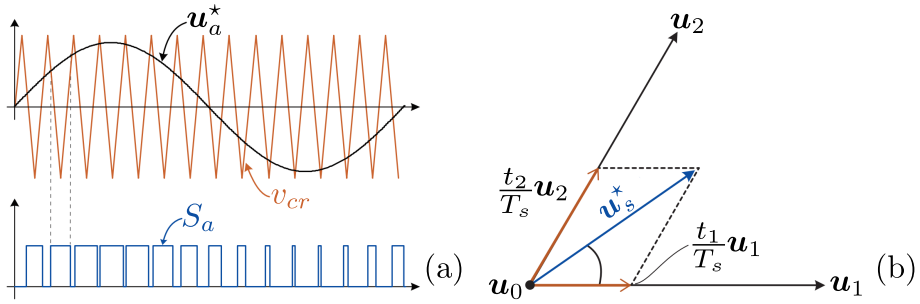


Figure 2.4: Pulse-Width Modulation strategies used in DC-AC Converters: (a) CB-PWM, and (b) SVM (taken from [63]).

Three types of VSC control schemes have been identified in the literature [63]. An open-loop scheme does not need measurements, see Fig. 2.5(a). It takes the reference vector and generates the appropriate switching signals to synthesize it at the output terminals. Due to the lack of measurements, open-loop schemes cannot attenuate disturbances in the plant. CB-PWM and SVM are examples of open-loop modulation schemes. On the other hand, closed-loop schemes use system measurements to take corrective action on the trajectory of the manipulated system, see Fig. 2.5(b). An example of closed-loop schemes is Field-Oriented Control (FOC) [65]. Finally, Direct methods are closed-loop schemes that do not need a modulator to generate the switching signals, see Fig. 2.5(c). For example, OSV-MPC [47], M^{2}PC [49], OSS-MPC [50], and hysteresis control [66] are direct modulation methods.

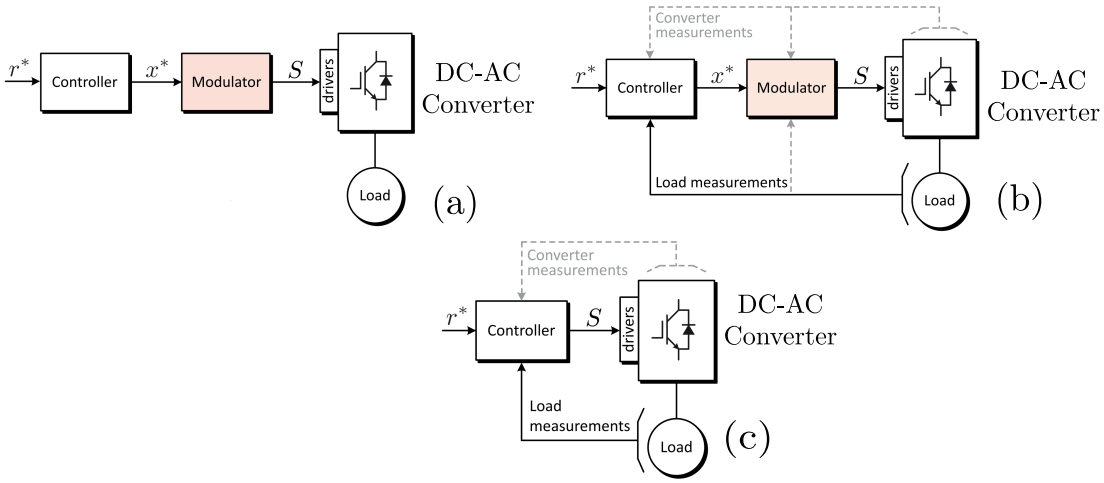


Figure 2.5: Three types of VSC control schemes. (a) Open-loop operation, (b) Closed-loop operation, and (c) Direct modulation (taken from [63]).

2.2.1. Carrier-Based PWM

CB-PWM compares a low-frequency sinusoidal signal and a high-frequency triangular signal [67]. Low-frequency sinusoids receive the name of modulation signals, while high-frequency triangular signals are called carrier signals. The switches in one leg are turned on and off when the modulation signal is greater or smaller than the carrier signal. Consider, for example, a 2L-VSI. The operation of CB-PWM for one leg of the 2L-VSI is shown in Fig. 2.4(a). This converter can generate two output voltage levels at its phase-to-neutral output terminals. Therefore, each leg has only two states. The PWM schemes only need one carrier signal to synthesize the modulation signal for each leg. When the amplitude of the modulation signal is greater than the carrier signal, the leg is connected to the positive rail of the DC-link. In the opposite case, when the amplitude of the modulation signal is smaller than the carrier signal, the leg is connected to the negative rail of the DC-link.

Carrier-based PWM for 3L-NPC converters uses two carrier signals in phase but displaced in the vertical axis [68]. The operation of CB-PWM for one leg of the 3L-NPC can be seen in Fig. 2.6. The range of the upper carrier signal is the interval [0, 1]. Meanwhile, the range of the lower carrier signal is [-1, 0]. As with the 2L-VSI, the leg switching state depends on the comparison of the modulation signal and the two carrier signals. When the amplitude of the modulation signal is greater than the upper carrier signal, the leg is connected to the positive rail of the DC-link. In the opposite case, when the amplitude of the modulation signal is smaller than the lower carrier signal, the leg is connected to the negative rail of the DC-link. The intermediate point, when the leg is connected to neutral-point of the DC-link, occurs when the modulation signal is smaller than the upper carrier and greater than the lower carrier [58].

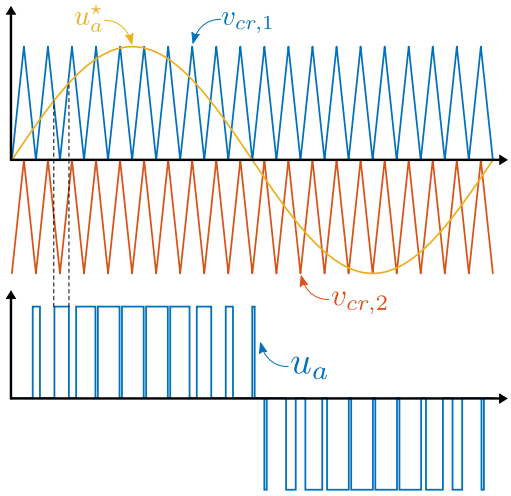


Figure 2.6: Carrier-Based PWM strategy for the 3L-NPC.

2.2.2. Space Vector PWM

SVM is a PWM method which uses a vectorial representation of the VSC in the stationary reference plane [63]. As stated before, the 3L-NPC has 19 non-redundant switching vectors and 8 redundant switching vectors in the the $\alpha\beta$ plane. In Fig. 2.7(a), all switching vectors of the 3L-NPC are shown. These vectors can be classified based on their length into four groups [60]:

- Zero vector ($\boldsymbol{u}_0$): There are three zero vectors. They are generated from the switching vectors $\begin{bmatrix}0 & 0 & 0\end{bmatrix}^\intercal$, $\begin{bmatrix}1 & 1 & 1\end{bmatrix}^\intercal$, and $\begin{bmatrix}-1 & -1 & -1\end{bmatrix}^\intercal$. Their magnitude is zero. In Fig. 2.7(a) is the black vector located at the center of the diagram.
- Small vectors ($\boldsymbol{u}_{s1}$-$\boldsymbol{u}_{s6}$): Red vectors in Fig. 2.7(a). They have an amplitude of 1/3.
- Medium vectors ($\boldsymbol{u}_{m1}$-$\boldsymbol{u}_{m6}$): Green vectors in Fig. 2.7(a). They have an amplitude of $\sqrt{3}/3$.
- Large vectors ($\boldsymbol{u}_{\ell 1}$-$\boldsymbol{u}_{\ell 6}$): Blue vectors in Fig. 2.7(a). They have an amplitude of 2/3.

SVM generate the gating signals for the converter switching devices computing a sequence of switching vectors and the length of time during which each is applied. The length of time to apply a switching vector is called dwell time. To simplify the computation of the dwell times, the space of vectors is divided in six triangular sectors (I to VI) with four triangular regions each ($\mathcal{R}_1$-$\mathcal{R}_4$) [60]. A reference vector will fall upon any region in one the six sectors. This reference vector will be synthesized by the three switching vectors that shape the sector in which it fell. Vectors farther away can be used as well, however, that will cause higher harmonic distortion in the converter output voltage [60].

Consider the case in 2.7(b), the desired vector $\boldsymbol{u}_s^\star$ falls in region 2 of sector I. The three nearest vectors to $\boldsymbol{u}_s^\star$ are $\boldsymbol{u}_{s1}$, $\boldsymbol{u}_{s2}$, and $\boldsymbol{u}_{m1}$. The modulation is based on the volt-second balancing principle. It means that the product of the reference vector and the sampling period T_s is equal to the linear combination of the switching vectors and their corresponding dwell times. Also, the sum of the switching vectors dwell times must be equal to the sampling period. Then, the following problem must be solved to find the dwell times of each vector:

$$\boldsymbol{u}_{s1}T_{s1} + \boldsymbol{u}_{s2}T_{s2} + \boldsymbol{u}_{m1}T_{m1} = \boldsymbol{u}_s^\star T_s \tag{2.6a}$$

$$T_{s1} + T_{s2} + T_{m1} = T_s \tag{2.6b}$$

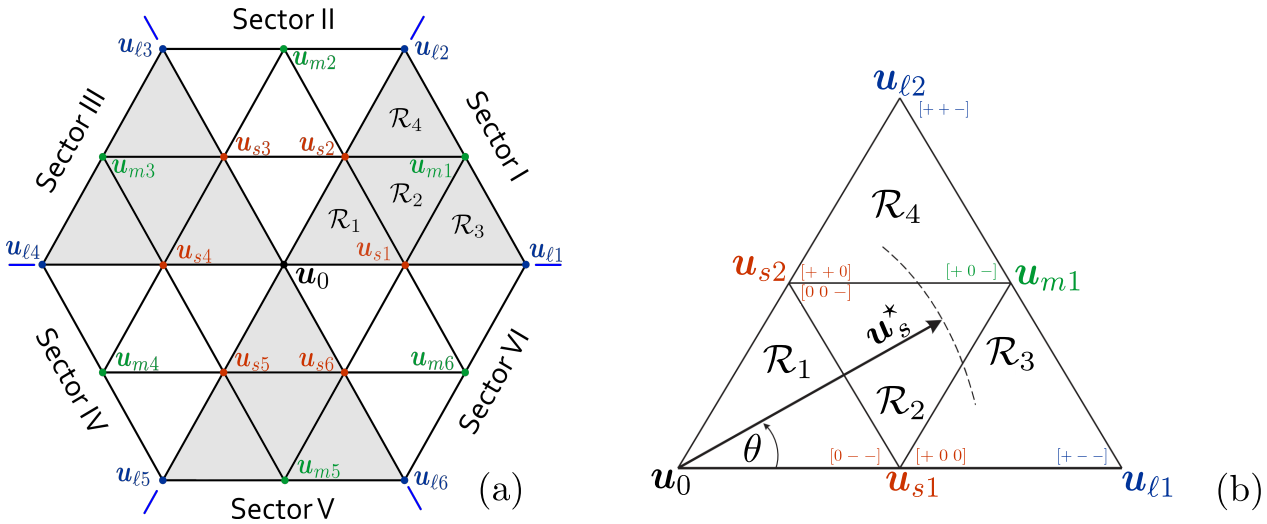


Figure 2.7: 3L-NPC Space of Vectors. (a) 3L-NPC switching vectors in the $\alpha\beta$ plane, and (b) reference vector moving through sector I in the $\alpha\beta$ plane.

The next problem is to design a switching sequence (i.e., determine an order for the switching vectors $\boldsymbol{u}_{s1}$, $\boldsymbol{u}_{s2}$, and $\boldsymbol{u}_{m1}$ to be applied). The design of the switching sequence can be

regarded as another degree of freedom in controller design. One example is Discontinuous Pulse-Width Modulation (DPWM). In DPWM, one phase is clamped to the negative DC rail for 120° of the fundamental period, while the other two phases change states [51]. The goal is to reduce the switching frequency; consequently reducing the converter power losses and improving converter efficiency. Another example is even-order harmonic elimination. Grid codes impose stringent requirements over even-order harmonics [69]. Thus, to comply with grid codes, a switching sequence is designed to provide half-wave symmetry for the converter output voltage and eliminate even-order harmonics from it [60]. In summary, switching sequence design can be used to achieve specific secondary control requirements.

Switching sequence design can be used to achieve DC-link neutral point voltage balance. Consider the circuit configurations shown in Fig. 2.8 and assume $i_a + i_b + i_c = 0$. In Fig. 2.8(a), a zero vector is applied (for example, vector $\begin{bmatrix}1 & 1 & 1\end{bmatrix}^\intercal$). Then, the neutral current $i_n = |1|i_a + |1|i_b + |1|i_c = 0$ (see eq. (2.4)). Thus, zero vectors do not affect the neutral-point voltage. In the same manner, large vectors do not affect the neutral-point voltage. If, for example, the large vector $\begin{bmatrix}1 & -1 & -1\end{bmatrix}^\intercal$ were to be applied to the system (see Fig. 2.8(e)) then the neutral current would be $i_n = |1|i_a + |-1|i_b + |-1|i_c = 0$.

Those vectors who bear influence over the neutral-point potential are the small and medium switching vectors. The influence cast by the medium switching vectors is, whoever, undetermined (it depends on the converter operating condition [70], see Fig. 2.8(d)). On the other hand, small vectors affect directly the neutral-point voltage. These vectors are produced by two different vectors in the natural reference frame, hence they have the property of redundancy. To understand the impact of small vectors is helpful to classify them as P-type and N-type vectors. P-type small vectors connect the output to the positive rail of the DC-link (see 2.8(b)), while N-type vectors connect it to the negative rail of the DC-link (see 2.8(c)). For instance, the small vector $\boldsymbol{u}_{s3}$ can be produced by $\boldsymbol{u}_{abc}=\begin{bmatrix}1 & 0 & 0\end{bmatrix}^\intercal$ (P-type small vector) or $\boldsymbol{u}_{abc}=\begin{bmatrix}0 & -1 & -1\end{bmatrix}^\intercal$ (N-type small vector), which according to (2.4), produce $i_n{=}i_a$ and $i_n{=}-i_a$, respectively. Thus, small vectors produce opposing effects over the neutral-point voltage.

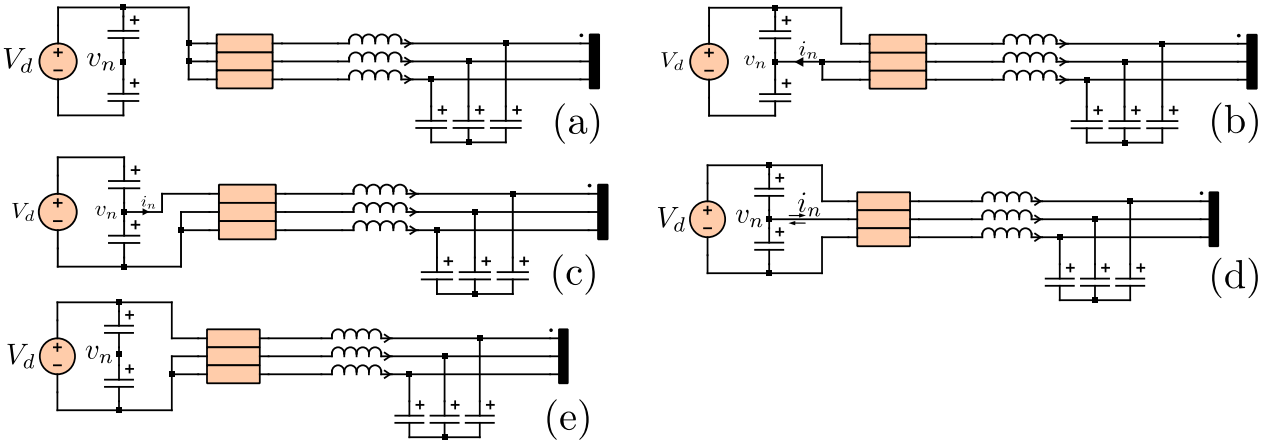


Figure 2.8: Circuit configuration when different switching vectors are applied. (a) zero vector, (b) P-type small vector, (c) N-type small vector, (d) medium vector, and (e) large vector.

The problem of neutral-point voltage balance has been studied in [70]. The paper concluded that the neutral-point can be balanced adjusting the relative duration of the P-type

and N-type small vectors in the switching sequence. In [60], two switching sequences for neutral-point balancing were proposed. Type-A switching sequence (see Fig. 2.9(a)) begin with an N-type small vector and end the sub-cycle period with an P-type small vector. On the contrary, B-type switching sequences (see Fig. 2.9(b)) begin with a P-type small vector and end the sub-cycle period with an N-type small vector.

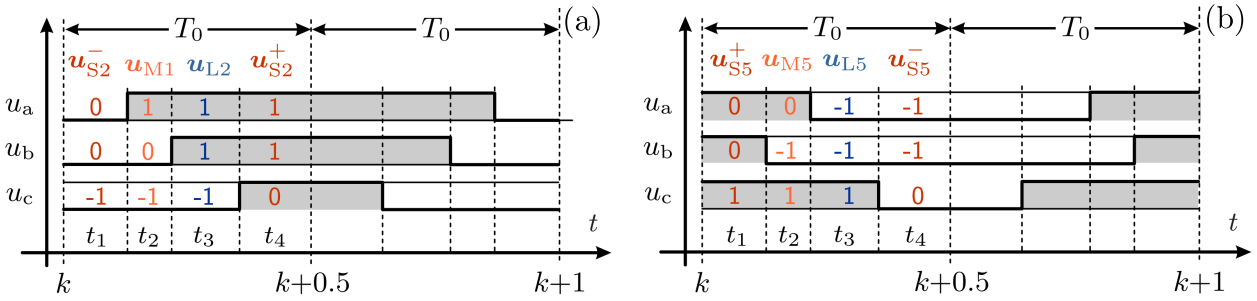


Figure 2.9: Two valid switching sequences: (a) Type-A Switching Sequence, and (b) Type-B Switching Sequence (taken from [62]).

The only difference between type-A switching sequence and type-B switching seequence is a time-shift equal to half sampling time of the PWM scheme. However, these switching sequences can be used alternatively to provide even-order harmonic elimininationin the converter output voltage waveforms [71].

2.3. Model Predictive Control for 3L-NPC

2.3.1. General operational principle of MPC

Model predictive control refers to a wide class of controllers, as discussed in the introduction (see Fig. 1.5 for a classification of MPC algorithms in power electronics). MPC algorithms use the model of the system to predict its future state, and choose the best possible actuation to be applied at the next sampling interval. The three common elements of MPC strategies are: the mathematical model of the plant, the optimization problem, and the receding horizon policy [37]. In this subsection, the general operational principle of MPC will be described briefly.

As mentioned, MPC use the model of the system for predictions. Lets consider the block diagram of an MPC algorithm shown in Fig. 1.4. In the diagram, the converter sends a signal $\boldsymbol{u}(t) \in \mathbb{U}$ as input to a plant. From the perspective of the control problem, the input to the plant can be either the switching signals of the converter, the duty cycles or the modulation signals. The plant then takes this input and generate an output $\boldsymbol{y}(t)$. The relationship between input and output can be described by a continuous-time mathematical model. The mathematical model has the form [37]:

$$\begin{aligned} \frac{d\boldsymbol{x}(t)}{dt} &= \boldsymbol{f}_c\left(\boldsymbol{x}(t), \boldsymbol{u}(t)\right) \\ \boldsymbol{y}(t) &= \boldsymbol{g}_c\left(\boldsymbol{x}(t)\right) \end{aligned} \tag{2.7}$$

where $\boldsymbol{x}(t) \in \mathbb{R}^{n_x}$ is the state vector, $\boldsymbol{y}(t) \in \mathbb{R}^{n_y}$ is the output vector, $\boldsymbol{f}_c(\star) : \mathbb{R}^{n_x} \times \mathbb{U} \rightarrow \mathbb{R}^{n_x}$ is the state-update function, and $\boldsymbol{g}_c(\star) : \mathbb{R}^{n_x} \rightarrow \mathbb{R}^{n_y}$ is the output function.

The control algorithm is executed in a digital hardware platform [42]. Therefore, the mathematical model of the plant need to be discretized. Usually, the discretization is done with one of three methods: forward Euler, backward Euler, or exact discretization [41, 44]. Forward and backward Euler are computationally cheap methods but they are less accurate than exact discretization. Exact discretization produce better predictions but at a higher computational load and only for linear time-invariant systems [37]. After discretization, the mathematical model of the plant has the form:

$$\boldsymbol{x}(k+1) = \boldsymbol{f}\left(\boldsymbol{x}(k), \boldsymbol{u}(k)\right) \tag{2.8a}$$

$$\boldsymbol{y}(k) = \boldsymbol{g}(\boldsymbol{x}(k)) \tag{2.8b}$$

where $k \in \mathbb{N}^+$ is the discrete time-step.

The discrete-time model is used to predict the future values of the system (i.e., $\boldsymbol{x}(k+1)$) based on measurements $\boldsymbol{x}(k)$ and the input $\boldsymbol{u}(k)$. In MPC, a sequence of input signals $\boldsymbol{U}(k)$ that span a large horizon is applied to the system (2.8a). The sequence $\boldsymbol{U}(k)$ can be defined as follows:

$$\boldsymbol{U}(k) = \begin{bmatrix} \boldsymbol{u}^\intercal(k) & \boldsymbol{u}^\intercal(k+1) & \dots & \boldsymbol{u}^\intercal(k+N_p-1) \end{bmatrix}^\intercal \tag{2.9}$$

where N_p is the prediction horizon of the algorithm. Using (2.8) and (2.9), the future states and outputs of the system can be predicted over the complete prediction horizon. The sequence of predicted outputs, $\boldsymbol{Y}(k)$, is defined as:

$$\boldsymbol{Y}(k) = \begin{bmatrix} \boldsymbol{y}^\intercal(k+1) & \dots & \boldsymbol{y}^\intercal(k+N_p) \end{bmatrix}^\intercal \tag{2.10}$$

Then, the predicted output values are compared against the desired output vector $\boldsymbol{Y}_{ref}(k) = \begin{bmatrix} \boldsymbol{y}_{ref}^\intercal(k+1) & \dots & \boldsymbol{y}_{ref}^\intercal(k+N_p) \end{bmatrix}^\intercal$ inside a cost function. The cost function J is used to map the control objectives into a non-negative scalar value [48], and it has the form:

$$J(\boldsymbol{x}(\ell), \boldsymbol{U}(k)) = \sum_{\ell=k}^{k+N_p-1} \|\boldsymbol{y}_{ref}(\ell+1) - \boldsymbol{y}(\ell+1)\|_p^p + \lambda_u \|\Delta \boldsymbol{u}(\ell)\|_p^p \tag{2.11}$$

where $p \in \{1, 2\}$ indicates the vector norm used. To define the ℓ_1-norm and ℓ_2-norm, lets consider the n-dimentional vector $\boldsymbol{\zeta} = \begin{bmatrix} \zeta_1 & \dots & \zeta_n \end{bmatrix}$. The ℓ_1-norm is defined as $\|\boldsymbol{\zeta}\|_1^1 = |\zeta_1| + \ldots + |\zeta_n|$, with $|\star|$ being the absolute-value function. The ℓ_2-norm is defined as $\|\boldsymbol{\zeta}\|_2^2 = \zeta_1^2 + \ldots + \zeta_n^2 = \boldsymbol{\zeta}^\intercal \boldsymbol{\zeta}$.

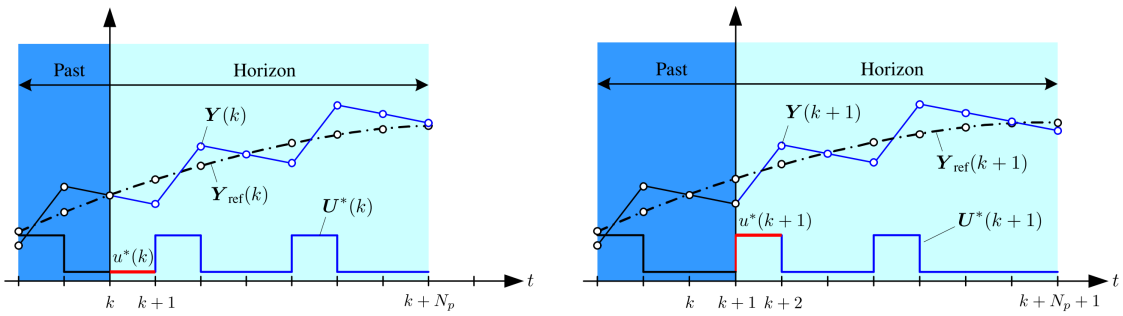
Choosing the norm for the cost function is an issue that has been discussed in the literature. In [43], it is considered that ℓ_1-norm and ℓ_2-norm do not produce significantly different results. In fact, ℓ_1-norm is selected because of its simplicity and reduced computational cost. In [44], the authors have agreed with the latter afirmation only when one variable is considered in the cost function. However, they state that ℓ_2-norm has better performance than ℓ_1-norm when the multivariable case is considered. Finally, in [48], it has been shown through a case study that ℓ_2-norm give better system performance.

In MPC, an optimization problem is solved at every time-step. The previosly defined cost function is used to choose the best available sequence of inputs to be applied to the converter. The optimal input sequence $\boldsymbol{U}^\star(k)$ is the one that minimize (2.11) in the following problem:

$$\begin{aligned} \boldsymbol{U}^{\star}(k) = \underset{\boldsymbol{U}(k)}{\text{minimize}} \quad & J\left(\boldsymbol{x}(k), \boldsymbol{U}(k)\right) \\ \text{subject to} \quad & \boldsymbol{u}(\ell) \in \mathbb{U} \\ & \boldsymbol{x}(\ell+1) \in \mathcal{X} \subseteq \mathbb{R}^{n_x} \\ & \forall \ell \in \{k, \ldots, k+N_p-1\} \end{aligned} \tag{2.12}$$

The variables in the optimization problem (2.12) can be subjected to soft and hard constraints [37]. Hard constraints are device-specific like the allowed switching states for the converter. Meanwhile, soft constraints are limits imposed on the system variables like maximum and minimum voltage or current values.

When the optimal solution $\boldsymbol{U}^{\star}(k)$ is found, it is applied following a receding horizon policy. Consider Fig. 2.10(a), if the solution found at time-step k were to be applied during the complete prediction horizon then the system would be susceptible to disturbances. During the period $[k, k+N_p]$, the system is operating in open-loop, without knowledge about the real value of its variables. For that reason, the receding horizon policy consist in applying only the first element of the optimal input sequence, discard the rest, and compute a new optimal sequence at each time-step (see Fig. 2.10(b)). The receding horizon policy adds feedback to the MPC control loop.



(a) Horizon at time-step k

(b) Horizon at time-step $k+1$

Figure 2.10: Receding horizon policy of direct MPC for a single-input single-output (SISO) system. A six-step prediction horizon ($N_p = 6$) is assumed. (figure taken from [37]).

The lenght of the prediction horizon is a tuning parameter in the MPC algorithm. Long prediction horizons can significantly improve the steady-state performance of the system [72]. However, the computational complexity increases exponentially with the horizon length and number of candidate solutions [37]. For example, lets consider the three-phase three-level NPC inverter. The number of candidate solutions considering a prediction horizon length of N_p is 3^{3N_p}, and the optimization variable will have $3N_p$ elements. Thus, for $N_p = 2$ the algorithm would have to search between 729 possible candidate solutions. Some algorithms, such as sphere decoding [73, 74], have been developed to tackle the issue of high computational complexity for long prediction horizon. A more detailed survey of algorithms for this problem can be found in [75]. Usually, a short prediction horizon ($N_p = 1$) is used to narrow the computational load [76].

2.3.2. Direct MPC algorithms for the 3L-NPC

OSV-MPC was first applied to the 3L-NPC for current control in a resistive-inductive-active load representing an induction machine [77]. In this strategy, the algorithm will search for the best possible switching vector to be applied during the next sampling period [78]. As mentioned before, the length of the prediction horizon in MPC for power converters is usually $N_p = 1$. Then, the input sequence is reduced to $\boldsymbol{U}(k) = \boldsymbol{u}_{abc}(k)$. In Fig. 2.11(a), the system under study is shown. The control objectives of the strategy are three: (1) reference tracking of the output current, (2) balance the DC-link capacitors voltages, and (3) minimize the converter switching frequency. The cost function designed to fulfill these objetives is the following:

$$J = |\boldsymbol{i}_o(k+1) - \boldsymbol{i}_o^{ref}| + \lambda_{dc}|\Delta V_{dc}| + \lambda_n n_c \tag{2.13}$$

where λ_{dc} and λ_n are the weigthing factors used to define the relevance of DC-link voltage balancing and switching frequency reduction to the optimization problem, and $\boldsymbol{i}_o(k+1)$ is the vector of predicted output current. A higher value of λ_{dc}, for example, will severely punish the switching vector that produce a high voltage deviation in the DC-link. In the paper, variable n_c is defined to track the number of commutations between the switching vector currently being applied to the converter, and the switching vector being evaluated (i.e., $n_c = |\Delta \boldsymbol{u}(k+1)| = |\boldsymbol{u}(k+1) - \boldsymbol{u}(k)|$). $\Delta V_{dc} = V_{c1}(k+1) - V_{c2}(k+1)$ is the voltage difference between the DC-link capacitors. The discrete-time model of the DC-link capacitor voltages use the current through each capacitor to predict its future value. The capacitor currents is defined as [79]:

$$i_{c1}(k) = i_{dc}(k) - H_{1a}i_a(k) - H_{1b}i_b(k) - H_{1c}i_c(k) \tag{2.14a}$$

$$i_{c2}(k) = i_{dc}(k) + H_{2a}i_a(k) + H_{2b}i_b(k) + H_{2c}i_c(k) \tag{2.14b}$$

Functions H_{1x} and H_{2x} are dependent on the state of the converter switching devices. $H_{1x} = 1$ when $u_x = 1$, otherwise its value is zero. In the same manner, $H_{2x} = 1$ when $u_x = -1$. Meanwhile, the DC-link capacitor voltages are defined as:

$$\begin{bmatrix} V_{c1}(k+1) \\ V_{c2}(k+1) \end{bmatrix} = \begin{bmatrix} V_{c1}(k) \\ V_{c2}(k) \end{bmatrix} + \frac{T_s}{C} \begin{bmatrix} i_{c1}(k) \\ i_{c2}(k) \end{bmatrix} \tag{2.15}$$

This prediction model for the DC-link capacitor voltages has been commonly used in predictive control of 3L-NPC converters [80, 81, 82]. In Fig. 2.11(b), the block diagram of the proposed current control strategy is shown. Notice that the strategy evaluates the cost function (2.13) for all the possible converter switching states. Thus, the strategy have a high computational burden.

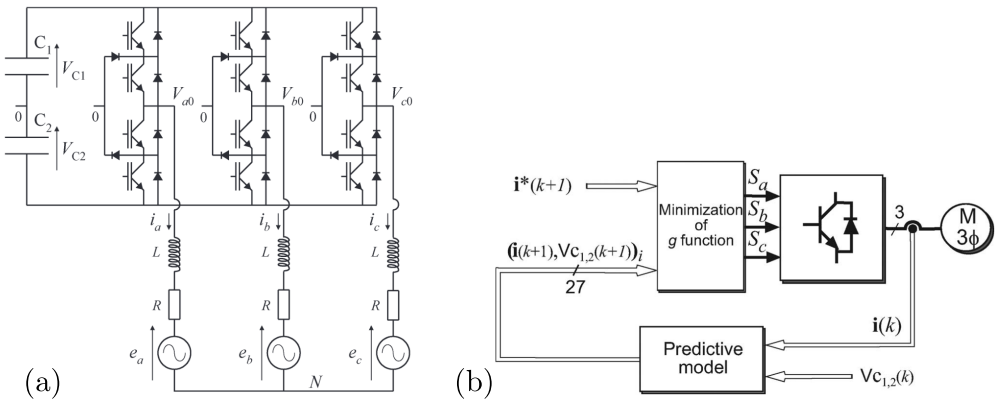


Figure 2.11: Current control of the 3L-NPC. (a) Converter topology and load, and (b) block diagram of the proposed predictive control strategy. (taken from [77]).

Some drawbacks of the strategy are:

- Use of ℓ_1-norm in a multivariable cost function.
- Variable switching frequency.
- High computational load.

In [83], a predictive current control scheme with less computational load is proposed. The same system shown in Fig. 2.11(a) is studied. In this case, the candidates switching vectors evaluated in the cost function are selected from a smaller hexagon in the space of vectors, as shown in Fig. 2.12(a). This allows the algorithm to evaluate 7 switching vectors instead of 27, as shown in the block diagram of Fig. 2.12(b). However, only one switching vector is applied to the converter. Thus, the strategy still suffer from a variable switching frequency.

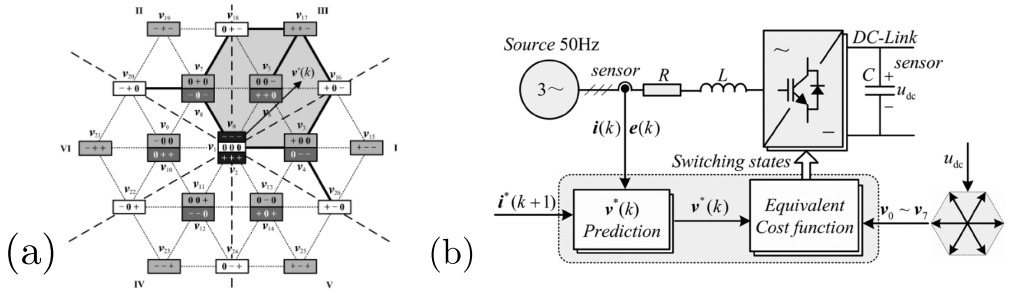


Figure 2.12: Simplified predictive current control for a 3L-NPC. (a) Space of vectors with smaller hexagon, and (b) block diagram of the proposed predictive control strategy. (taken from [83]).

Variable switching frequency is an issue in grid-connected converters due to the stringent requirements imposed by grid codes and the difficulty of designing filters [48]. In [82], two M^{2}PC strategy for grid-connected 3L-NPC were proposed (see Fig. 2.13(a)). M^{2}PC computes a sequence of switching vectors and their corresponding application times to be applied during the next sampling period. The control strategy behaves like an SVM strategy (it is classified under the category of MPC with implicit modulators in Fig. 1.5). The input sequence $\boldsymbol{U}(k)$ for this scheme is the sequence of switching vectors $\boldsymbol{S}(k)$ defined as follows:

$$\boldsymbol{S}(k) = \{\underbrace{v_{1j}}_{\frac{d_{1j}}{2}}, \underbrace{v_{2j}}_{\frac{d_{2j}}{2}}, \underbrace{v_{3j}}_{d_{3j}}, \underbrace{v_{2j}}_{\frac{d_{2j}}{2}}, \underbrace{v_{1j}}_{\frac{d_{1j}}{2}}\} \tag{2.16}$$

Where d_{ij} with $i \in \{1, 2, 3\}$ are the duty cycles of each vector in the sequence. The strategies proposed in the paper differ in the method to balance the DC-link capacitors voltages. The first strategy includes the voltages of the DC-link capacitors into the cost function (as done in (2.13)). The prediction model for the DC-link capacitor voltages is (2.15). The second strategy use the redundant small vectors of the converter to balance the capacitor voltages. Thus, the cost function of the M^{2}PC problem is used only for grid-current tracking. In Fig. 2.13(b), the block diagram of the proposed control strategies is shown.

Both strategies solve the optimization problem in two stages: the first stage computes the sequence of switching vectors that minimize the cost function. Meanwhile, the second stage use the cost function associated to each switching vector to compute their duty cycles. The duty cycles are computed as follows:

$$d_{1j} = \frac{g_{2j}g_{3j}}{g_{1j}g_{2j} + g_{2j}g_{3j} + g_{3j}g_{1j}} \tag{2.17a}$$

$$d_{2j} = \frac{g_{1j}g_{3j}}{g_{1j}g_{2j} + g_{2j}g_{3j} + g_{3j}g_{1j}} \tag{2.17b}$$

$$d_{3j} = \frac{g_{1j}g_{2j}}{g_{1j}g_{2j} + g_{2j}g_{3j} + g_{3j}g_{1j}} \tag{2.17c}$$

where g_{ij} are the cost functions associated to each vector in the candidate switching sequence. The cost function is defined as:

$$g_{ij} = \|\boldsymbol{i}_o(k+1) - \boldsymbol{i}_o^*\|_2^2 \tag{2.18}$$

with $\boldsymbol{i}_g(k+1)$ being the prediction vector of the grid current, and $\boldsymbol{i}_g^*$ being the vector of desired grid current.

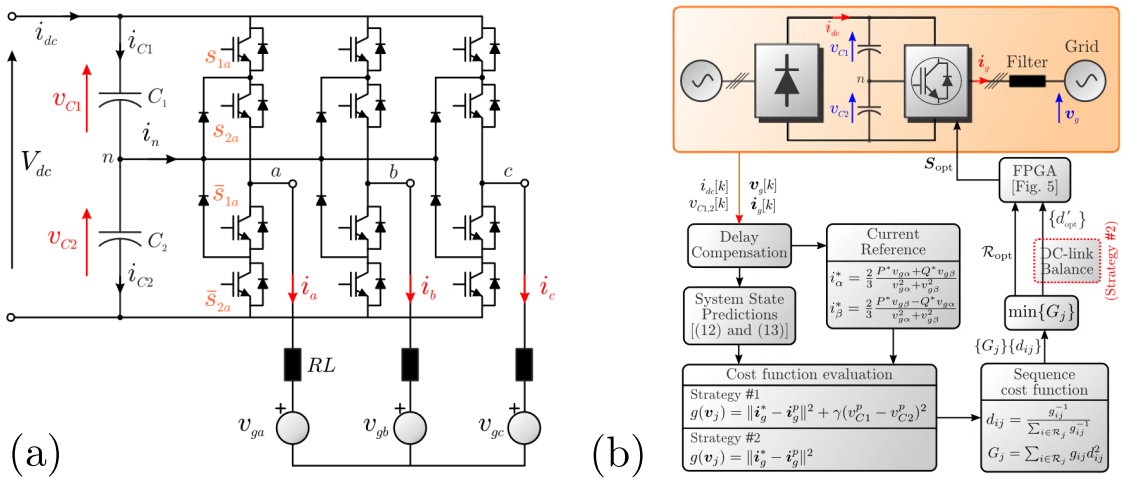


Figure 2.13: M^{2}PC current control for a 3L-NPC. (a) System under study, and (b) block diagram of the proposed predictive control strategies. (taken from [82]).

In [53], a predictive current control based on the concept of optimal switching sequence is proposed. The system under study is a grid-connected 3L-NPC such as in Fig. 2.13(a). The strategy solves two constrained optimization problem (one for the grid current and other for the DC-link voltages). The solution to the grid current optimization problem are the sequence of switching vectors and their duty cycles. Then, the duty cycles of the small vectors is optimally distributed between them to achieve balance in the DC-link capacitor voltages. The strategy is then extended for direct power control in [55]. In that paper, a new DC-link voltage balancing scheme based on injecting an optimal zero sequence voltage to the converter modulation signals is introduced. The block diagram of both OSS-MPC strategies is shown in Fig. 2.14.

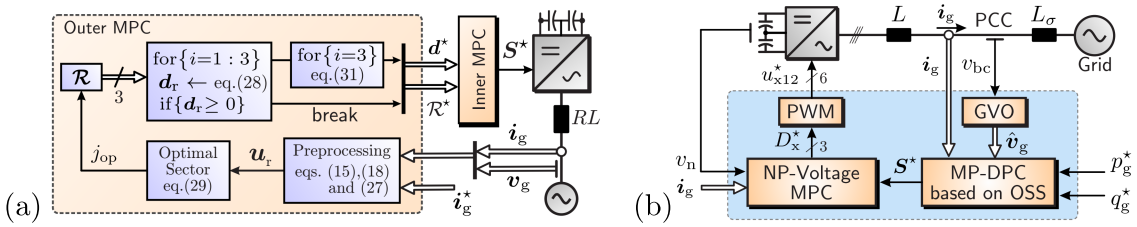


Figure 2.14: OSS-MPC current and direct power control for the 3L-NPC. (a) Block diagram of C-OSS-MPC for grid-current control (taken from [53]), and (b) block diagram of C-OSS-MPC direct power control for the 3L-NPC. (taken from [55]).

2.3.3. Predictive Voltage Control for 3L-NPC

Some predictive voltage control strategies for the 3L-NPC based on M^{2}PC has been proposed in the literature. In [27], the 3L-NPC converter is feeding a linear load through an LC filter. The system configuration is shown in Fig. 2.15(a). The control objectives for this system are two: (1) output voltage tracking, and (2) DC-link capacitor voltage balance. The cost function used in this work is the following:

$$J = \|\boldsymbol{v}_o(k+1) - \boldsymbol{v}_o^{ref}(k+1)\|_2^2 + \lambda_{dc}\|\Delta V_{dc}\|_2^2 \tag{2.19}$$

where $\boldsymbol{v}_o$ is the filter output voltage. In Fig. 2.15, the block diagram of the control strategy is shown. It can be seen that the control scheme computes the cost function for each possible switching sequence in the space of vectors of the 3L-NPC. Thus, 36 switching sequences are evaluated at each time-step. This may produce a high computational load for the algorithm. Also, the system performance is evaluated through simulations only for a resistive linear load connected at the output of the LC filter.

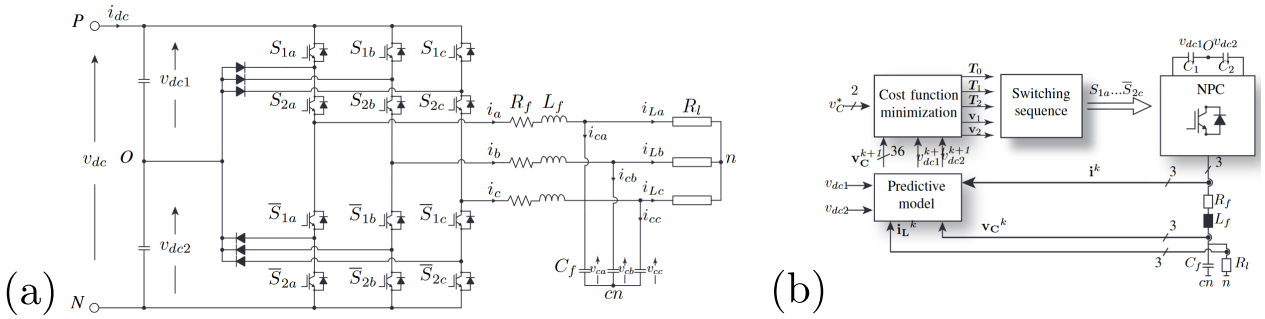


Figure 2.15: M^{2}PC-based predictive voltage control for the 3L-NPC. (a) System under study, and (b) block diagram of predictive voltage control strategy. (taken from In [27]).

In [30], other M^{2}PC-based predictive voltage control strategy is proposed. The system under study is the same as Fig. 2.15(a). The converter current and output voltage are controlled simultaneously to reduce cross-coupling between the state variables. Thus, the following multiobjetive cost function is used:

$$J = \|\boldsymbol{v}_o(k+1) - \boldsymbol{v}_o^{ref}(k+1)\|_2^2 + \lambda_i \|\boldsymbol{i}_f(k+1) - \boldsymbol{i}_f^{ref}(k+1)\|_2^2 + \lambda_{dc} \|\Delta V_{dc}\|_2^2 \tag{2.20}$$

where $\boldsymbol{v}_o$ is the filter output voltage, and $\boldsymbol{i}_f$ is the converter current. The performance of the strategy was tested in simulation for linear and nonlinear loads. The strategy computes the cost function for every possible switching vector of the 3L-NPC.

Drawbacks of the predictive voltage control strategies for the 3L-NPC:

- M^{2}PC control is used. This control strategy has suboptimal performance.
- Only simulation results are provided.
- DC-link voltages are balanced through the cost function. Then, the redundancy of the small switching vectors is not being used.
- Weight factor sintonization needed for DC-link voltage balancing.

Chapter 3

Cascaded Optimal Switching Sequence Model Predictive Control

The Cascaded Optimal Switching Sequence MPC (C-OSS-MPC) controller is a predictive control scheme based on the solution to two cascaded optimization problems. The first optimization problem —hereinafter called the outer optimization loop— computes the optimal switching vectors sequence and duty cycles that minimize a cost function. The cost function is designed to track the desired values of the state vector and minimize the control effort of the converter. The second optimization problem —hereinafter called the inner optimization loop— computes an optimal zero-sequence injection signal. The zero-sequence injection signal is designed to balance the neutral-point voltage between the DC-link capacitors.

This chapter describes a procedure to design the C-OSS-MPC scheme. The first section deals with the discretization of the plant to implement a discrete state-space system. The second section discusses the design of the reference state vector, and outer loop cost function. The third section presents the analytical solution to the outer optimization loop, distinguishing between two modes of operation: (1) linear modulation mode, and (2) overmodulation mode. Finally, the fourth section describes the solution for the inner optimization loop.

The 3L-NPC topology shown in Fig. 3.1 consist of three phases with active semicondutor devices and freewheeling diodes each. The phases are connected in parallel to produce a switched output voltage waveform from a DC voltage source. Two series-connected diodes connect the node between the upper-side and lower-side switching devices, allowing the converter to generate three-level output voltages. This feature reduce the THD of the output voltage waveform compared with classical two-level VSC's.

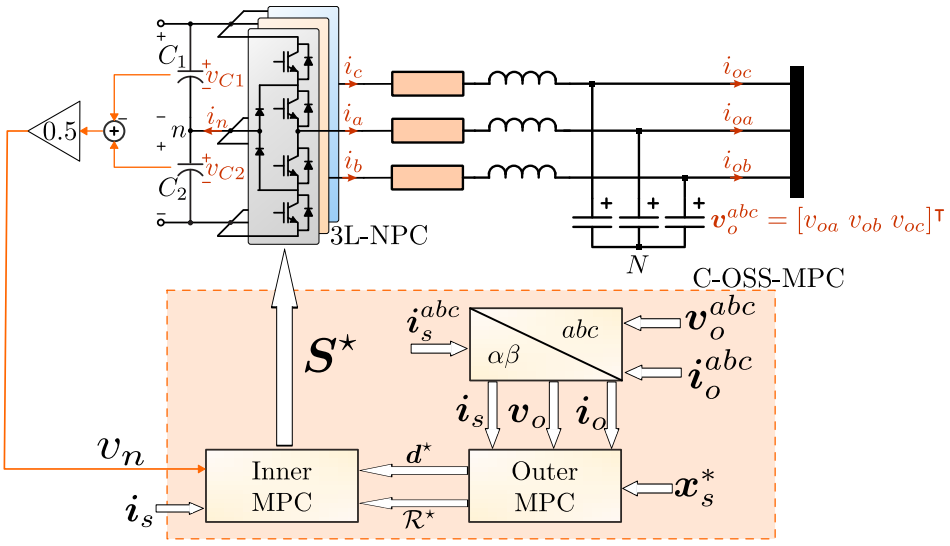


Figure 3.1: Electrical diagram of the plant and block diagram of the C-OSS-MPC strategy used to generate the optimal switching signals.

Each leg switching device is controlled by turn-on and turn-off signals. Then, the device switching state is either $\{off, on\}$ or $\{0, 1\}$ and can be represented by the variables u_{1x} and u_{2x}. The leg switching state summarizes the position of each active device in one of the legs. The discrete variable $u_x \in \{1, 0, -1\}$ represents the switching state for any of the converter legs. As mentioned before, the definition of the leg switching state is a set with three elements depicting the three possible states for the leg output voltage.

The switching vector $\boldsymbol{u}_{abc} = [u_a\ u_b\ u_c]^\intercal \in \mathbb{U} \triangleq \{1, 0, -1\}^3$ describes the behavior of all converter legs. The elements of the set $\mathbb{U}$ are 27 triplets that represent all possible switching combinations of the converter. The switching vector can be mapped to the $\alpha - \beta$ stationary reference frame using the transformation matrix $\boldsymbol{\mathcal{T}}$ defined by eq. (2.2). The transformation $\boldsymbol{u}_s = \boldsymbol{\mathcal{T}}\boldsymbol{u}_{abc} \in \mathcal{U} \triangleq \boldsymbol{\mathcal{T}}\mathbb{U}$ generates 19 non-redundant switching vectors and 8 redundant switching vectors in the stationary reference frame, as shown in Fig. 3.2(a). Redundant vectors are those who are mapped from different vectors in the *abc*-coordinate system to the same vector in the stationary reference frame.

The 3L-NPC Space of Vectors is divided into 6 triangular sectors, and each sector is divided in 4 triangular regions, see Fig. 3.2(a). There exist 24 regions $\mathcal{R}_j$ in the Space of Vectors. To Synthesize the desired output voltage during each switching cycle, the converter applies in order the three switching vectors nearest to the desired voltage. The three-nearest switching vectors are usually the vertices of the triangular region $\mathcal{R}_j$. The order of application of these vectors is called switching sequence (SS).

As mentioned in the previous chapter, switching sequences are designed to achieve secondary control objectives. In the particular case of this work, we follow the design guidelines given by [60]. The design requirements for the switching sequence are as follows: (i) the transition between two switching states involves only two active semiconductor devices in one leg, (ii) the commutations when the reference vector move from one sector (or region) to another must be minimized, and (iii) the switching state effect over the neutral-point voltage deviation has to be minimized. In this work, a N-type seven-segment switching sequence (7S-SS) will be used. The sequence starts with an N-type small vector and ends the subcycle with its P-type redundancy, as shown in Fig. 3.2(b). The 7S-SS can be defined accordingly as:

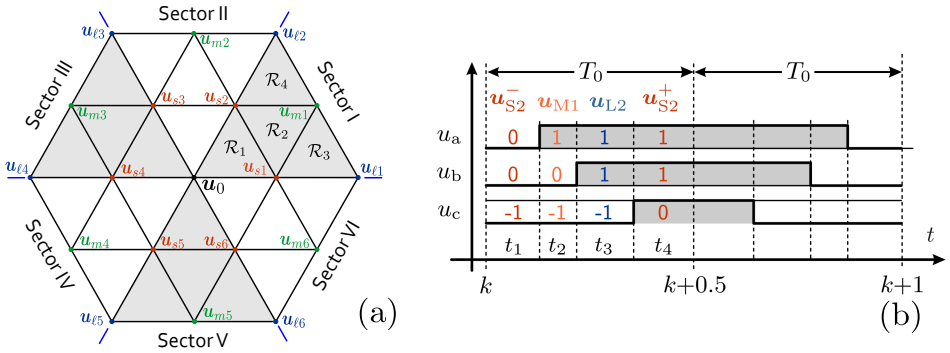


Figure 3.2: Space of Vectors and Switching Sequence for the 3L-NPC. (a) Space of Vectors, and (b) N-type 7S-SS.

$$\boldsymbol{S} := \left\{ \boldsymbol{u}_S^-[d_0], \boldsymbol{u}_1[d_1], \boldsymbol{u}_2[d_2], \boldsymbol{u}_S^+[d_3], \boldsymbol{u}_2[d_2], \boldsymbol{u}_1[d_1], \boldsymbol{u}_S^-[d_0] \right\} \tag{3.1}$$

Where d_i is the duty cycle of the ith switching vector in the sequence. In the next sections, the different elements of the C-OSS-MPC strategy will be designed.

3.1. Mathematical model of the LC filter

The LC filter is a second-order electrical system. These systems are formed by two storage elements: an inductor, and a capacitor. The electrical schematic of the LC filter used in this work is shown in Fig. 3.3.

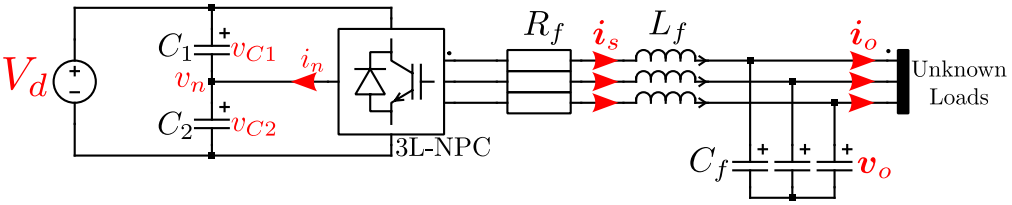


Figure 3.3: Diagram of the 3L-NPC connected to the LC filter to feed unknown loads.

3.1.1. Continuous-time model

The outer loop controller is designed assuming that the DC-link NP-voltage is balanced. Thus, the converter output voltage of (2.1) is equal to $\boldsymbol{v} = \frac{V_{dc}}{2}\boldsymbol{u}$.

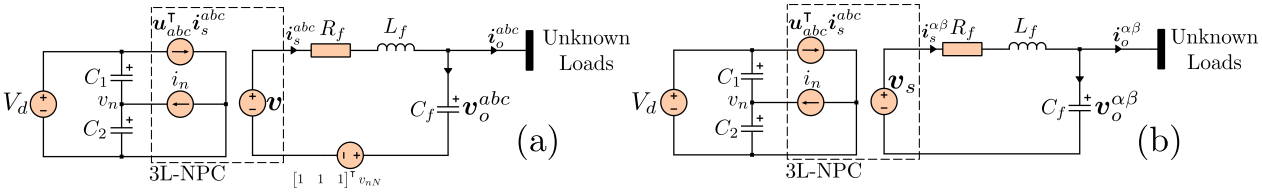


Figure 3.4: Equivalent circuit of the controlled system. (a) Natural reference frame model, (b) Stationary reference frame.

The state and disturbance vectors in abc reference frame are $\boldsymbol{x}_s^{abc} = [i_s^a\ i_s^b\ i_s^c\ v_o^a\ v_o^b\ v_o^c]^\intercal$, and $\boldsymbol{i}_o^{abc} = [i_o^a\ i_o^b\ i_o^c]^\intercal$, respectively. The dynamics of the AC side are modelled from the equivalent circuit of Fig. 3.4(a) where the converter has been replaced by a controllable voltage source. Applying Kirchhoff Voltage and Current law to the circuit we get the differential equations of the inductor and capacitor

$$\begin{aligned} L_f \frac{di_s^a}{dt} + R_f i_s^a &= v_a - v_o^a - v_{nN} \\ C_f \frac{dv_o^a}{dt} &= i_s^a - i_o^a \end{aligned} \tag{3.2}$$

This model is equivalent at the three-phases of the filter. The three-phase model is then written as

$$\begin{aligned} L_f \frac{d\boldsymbol{i}_s^{abc}}{dt} + R_f \boldsymbol{i}_s^{abc} &= \boldsymbol{v} - \boldsymbol{v}_o^{abc} - \mathbb{1}^\intercal v_{nN} \\ C_f \frac{d\boldsymbol{v}_o^{abc}}{dt} &= \boldsymbol{i}_s^{abc} - \boldsymbol{i}_o^{abc} \end{aligned} \tag{3.3}$$

The system is three-phase and balanced, thus the condition $x_a + x_b + x_c = 0$ holds. Therefore, we have a system with two independent variables and one dependent variable. The system is mapped to the α-β reference frame using the Amplitude Invariant Clarke Transformation defined in Chapter 2, see eq. (2.2). The system of differential equations describing the dynamics of the LC filter in the AC side of the converter (see Fig. 3.4(b)) is then

$$\begin{aligned} L_f \frac{d\boldsymbol{i}_s^{\alpha\beta}}{dt} + R_f \boldsymbol{i}_s^{\alpha\beta} &= \boldsymbol{v}_s - \boldsymbol{v}_o^{\alpha\beta} \\ C_f \frac{d\boldsymbol{v}_o^{\alpha\beta}}{dt} &= \boldsymbol{i}_s^{\alpha\beta} - \boldsymbol{i}_o^{\alpha\beta} \end{aligned} \tag{3.4}$$

Rearrange the equations and define the state, input and perturbance vectors as $\boldsymbol{x}_s = [i_s^\alpha\ i_s^\beta\ v_o^\alpha\ v_o^\beta]^\intercal$, $\boldsymbol{u}_s = [u_s^\alpha\ u_s^\beta]^\intercal$, and $\boldsymbol{i}_o = [i_o^\alpha\ i_o^\beta]^\intercal$ (The superscripts $\alpha\beta$ in the vectors will be avoided to simplify the notation). The state-space model of the AC side dynamics is then

$$\dot{\boldsymbol{x}}_s = \mathbf{A}\boldsymbol{x}_s + \mathbf{B}\boldsymbol{u}_s + \mathbf{E}\boldsymbol{i}_o \tag{3.5a}$$

$$\boldsymbol{y} = \mathbf{C}\boldsymbol{x}_s \tag{3.5b}$$

Matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{E}$ contains the parameters of the filter, and matrix $\mathbf{C}$ is the identity matrix.

$$\mathbf{A} = \begin{bmatrix} -\mathbf{L}^{-1}\mathbf{R} & -\mathbf{L}^{-1} \\ \mathbf{C}_f^{-1} & \mathbf{0} \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} \frac{V_{dc}}{2}\mathbf{L}^{-1} \\ \mathbf{0} \end{bmatrix} \qquad \mathbf{E} = \begin{bmatrix} \mathbf{0} \\ -\mathbf{C}_f^{-1} \end{bmatrix} \tag{3.6}$$

The resistance, inductance, and capacitance matrices are defined as follows:

$$\mathbf{R} = R_f\mathbf{I}_2 \quad \mathbf{L} = L_f\mathbf{I}_2 \quad \mathbf{C}_f = C_f\mathbf{I}_2 \tag{3.7}$$

The dimensions of the system matrices are $\mathbf{A} \in \mathbb{R}^{4\times4}$, $\mathbf{B} \in \mathbb{R}^{4\times2}$, $\mathbf{E} \in \mathbb{R}^{4\times2}$, $\boldsymbol{x}_s(t) \in \mathbb{R}^{4\times1}$, $\boldsymbol{u}_s(t) \in \mathbb{R}^{2\times1}$, and $\boldsymbol{i}_o(t) \in \mathbb{R}^{2\times1}$. The input-output relationship for (3.5) is given by the

transfer matrix $\mathbf{G}(s)$ which is defined as [84]:

$$\mathbf{G}(s) = \mathbf{C}\left(s\mathbf{I} - \mathbf{A}\right)^{-1}\mathbf{B} + \mathbf{D} \tag{3.8}$$

Considering $\mathbf{C} = \mathbf{I}_4$ and $\mathbf{D} = \mathbf{0}$, and matrices $\mathbf{A}$ and $\mathbf{B}$ defined in (3.7), the transfer matrix for the system is:

$$\mathbf{G}(s) = \frac{1}{\Delta(s)}\begin{bmatrix} \frac{V_{dc}}{2L_f}s\mathbf{I}_2 \\ \frac{V_{dc}}{2L_fC_f}\mathbf{I}_2 \end{bmatrix} \tag{3.9}$$

The characteristic equation for (3.5), $\Delta(s)$, is given by:

$$\Delta(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{3.10}$$

Coefficients ζ and ω_n are the damping ratio and natural frequency, respectively. They are defined based on the LC filter parameters:

$$\zeta = \frac{R_f}{2}\sqrt{\frac{C_f}{L_f}} \quad \omega_n = \frac{1}{\sqrt{L_fC_f}} \tag{3.11}$$

3.1.2. Discrete-time model

MPC uses the discrete-time mathematical model of the system to make predictions of the state vector trajectory, then uses the predicted values in an optimization problem and compute the best control action that fulfill the control objectives. In this section, two discrete-time approximation of the continuous-time model will be obtained using the forward Euler method and Heun's method (also known as improved Euler's method) [85].

The evolution of the state trajectory can be computed as increments using eq. (3.5a) and the vectors of the candidate switching sequence [50]. If we assume a small switching period T_s then the instantaneous state vector can be considered as a piecewise function of time and the switching vector applied to the converter (cf. [53]), as follows:

$$\left.\frac{d\boldsymbol{x}_s}{dt}\right|_{t=\ell} = m_\ell = f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right); \quad \forall\ell \tag{3.12}$$

where $\ell \in \{0, 1, 2, 3\}$ is the index for the switching vectors of the sequence. Traditionally, the state vector trajectory is computed for the complete switching cycle [44, 50], see Fig. 3.5(a). However, in [62] it was proved that the instantaneous evolution of the state vector at the end of the switching sub-cycle is equivalent to its average trajectory over the complete switching cycle when a symmetric switching sequence is used. In this work, the prediction model used will be the average value of the state vector trajectory over the switching sub-cycle (i.e., half switching cycle or $T_o = T_s/2$), as proposed by Mora et. al. [53, 62], see Fig. 3.5(b).

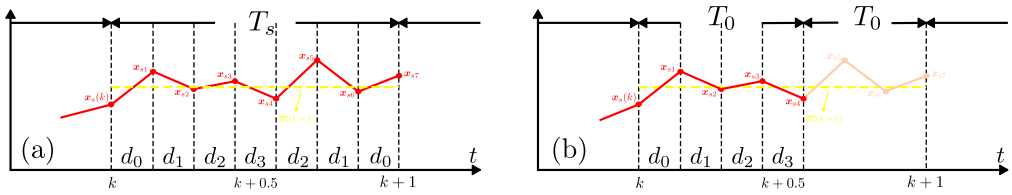


Figure 3.5: State trajectory for a 7S-SS. (a) State trajectory computed for the complete switching cycle, and (b) state trajectory computed for the switching sub-cycle.

3.1.2.1. Forward Euler-Based Discrete Time Model

Assume that a 7S-SS is applied to the converter during every switching cycle. Considering forward Euler's method, the instantaneous trajectory of the state vector when the ℓth switching vector is applied can be computed as:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + T_0 f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right) d_\ell \tag{3.13}$$

As previosly mentioned, the instantaneous evolution of the state vector prediction at the end of the sub-cycle corresponds to its average trajectory when the seven-segment SS defined by (3.1) is applied to the system:

$$\overline{\boldsymbol{x}}_s[k+1] = \boldsymbol{x}_s[k] + T_0 \sum_{\ell=0}^{3} \left.\frac{d\boldsymbol{x}_s}{dt}\right|_{t=\ell} d_\ell \tag{3.14}$$

where $T_0 = T_s/2$ is the sub-cycle period. To simplify the analysis, every subinterval slope m_ℓ is approximated using the values of the state and disturbance vector at the sampling instant k as $m_\ell \approx f(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k])$. Therefore, the prediction of the average trajectory can be expressed as:

$$\overline{\boldsymbol{x}}_s[k+1] = \mathbf{A}_d \boldsymbol{x}_s[k] + \mathbf{E}_d \boldsymbol{i}_o[k] + \mathbf{B}_d \sum_{\ell=0}^{3} \boldsymbol{u}_{s\ell} d_\ell \tag{3.15}$$

where $\mathbf{A}_d = \mathbf{I}_4 + T_0\mathbf{A}$, $\mathbf{E}_d = T_0\mathbf{E}$, and $\mathbf{B}_d = T_0\mathbf{B}$. Consider the linear combination of switching vectors and duty cycles at the end of eq. (3.15):

$$\sum_{\ell=0}^{3} \boldsymbol{u}_{s\ell} d_\ell = \boldsymbol{u}_{s0} d_0 + \boldsymbol{u}_{s1} d_1 + \boldsymbol{u}_{s2} d_2 + \boldsymbol{u}_{s3} d_3 \tag{3.16}$$

On the grounds that for any N-type seven-segment SS we have that $\boldsymbol{u}_{s0} = \boldsymbol{u}_S^- = \boldsymbol{u}_s$, and $\boldsymbol{u}_{s3} = \boldsymbol{u}_S^+ = \boldsymbol{u}_s$, then eq. (3.16) is simplified to:

$$\boldsymbol{u}_{s0} d_0 + \boldsymbol{u}_{s1} d_1 + \boldsymbol{u}_{s2} d_2 + \boldsymbol{u}_{s3} d_3 = \boldsymbol{u}_s (d_0 + d_3) + \boldsymbol{u}_{s1} d_1 + \boldsymbol{u}_{s2} d_2 \tag{3.17}$$

The duty cycles d_0 and d_3 can be combined as $d_s = d_0 + d_3$ which is the duty cycle for the small vectors of the sequence (cf. [53]). Then, the following linear representation of the average trajectory can be stated:

$$\overline{\boldsymbol{x}}_s[k+1] = \mathbf{A}_d \boldsymbol{x}_s[k] + \mathbf{E}_d \boldsymbol{i}_o[k] + \mathbf{B}_d \boldsymbol{U} \boldsymbol{d} \tag{3.18}$$

where the dwell-time vector $\boldsymbol{d}$ and switching matrix $\boldsymbol{U}$ are defined as:

$$\boldsymbol{d} = \begin{bmatrix} d_s & d_1 & d_2 \end{bmatrix} \in \mathbb{D} \triangleq [0,1]^3 \tag{3.19a}$$

$$\boldsymbol{U} = \begin{bmatrix} \boldsymbol{u}_s & \boldsymbol{u}_1 & \boldsymbol{u}_2 \end{bmatrix} \tag{3.19b}$$

3.1.2.2. Improved Euler-Based Discrete Time Model

Improved Euler's method is a second-order Runge-Kutta method to compute the solution of ordinary differential equations [85]. In this method, the weighted average of the approximations to the derivative at intermediate points on the solution curve is computed. Specifically, improved Euler's method use the extreme points of the solution interval (i.e., kth and $(k+1)$th points). Higher-order Runge-Kutta methods use more intermediate points to increase accuracy of the solution.

Once again, assume that a 7S-SS is applied by the converter during the complete switching cycle. Considering improved Euler's method, the instantaneous evolution of the state vector is given by the following equation:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + \frac{T_s}{2}\left[f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right) + f\left(\boldsymbol{x}_{s\ell}[k+1], \boldsymbol{u}_{s\ell}[k+1], \boldsymbol{i}_{o\ell}[k+1]\right) \right] d_\ell \tag{3.20}$$

The average slope is multiplied by T_s because it is the time-length between predictions in the interval $[k, k+1]$ and predictions in the interval $[k+1, k+2]$, see Fig. 3.6. The expression (3.20) is complex. To simplify it, we will make some assumptions about the states and inputs used for computation. First, the slope of the system at the kth time instant is computed with the values measured at time instant k (i.e., $f\left(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}\right) \approx f\left(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]\right)$). Second, the slope at time $(k+1)$th is computed with the average state vector $\overline{\boldsymbol{x}}_s[k+1]$ defined by (3.18), and the switching sequence applied is the same of time instant k (i.e., $f\left(\boldsymbol{x}_{s\ell}[k+1], \boldsymbol{u}_{s\ell}[k+1], \boldsymbol{i}_{o\ell}[k+1]\right) \approx f\left(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1]\right)$). The disturbance vector is assumed to be constant during the switching cycle, but different between switching cycles (i.e., $\boldsymbol{i}_o[k] \neq \boldsymbol{i}_o[k+1]$). Considering these assumptions, the state vector trajectory is described by:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + \frac{T_s}{2}\left[f\left(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]\right) + f\left(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1]\right) \right] d_\ell \tag{3.21}$$

The slopes $\boldsymbol{m}_\ell[k] = f\left(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]\right)$ and $\boldsymbol{m}_\ell[k+1] = f\left(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1]\right)$ are described by the following equations:

$$\boldsymbol{m}_\ell[k] = \mathbf{A}\boldsymbol{x}_s[k] + \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k] \tag{3.22a}$$

$$\boldsymbol{m}_\ell[k+1] = \mathbf{A}\overline{\boldsymbol{x}}_s[k+1] + \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k+1] \tag{3.22b}$$

The average prediction $\overline{\boldsymbol{x}}_s[k+1]$ is the one obtained using forward Euler method (see (3.18)). Replacing $\overline{\boldsymbol{x}}_s[k+1]$ in (3.22b), we get the expression for the slope $\boldsymbol{m}_\ell[k+1]$ as follows:

$$\begin{aligned}\boldsymbol{m}_\ell[k+1] = &\left(\mathbf{A} + T_0\mathbf{A}^2\right)\boldsymbol{x}_s[k] + T_0\mathbf{A}\mathbf{B}\boldsymbol{u}_j + T_0\mathbf{A}\mathbf{E}\boldsymbol{i}_o[k] \\ &+ \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k+1]\end{aligned} \tag{3.23}$$

Then, the average trajectory of the state vector using improved Euler method is computed as:

$$\overline{\boldsymbol{x}}_s[k+1] = \boldsymbol{x}_s[k] + \frac{T_s}{2}\sum_{\ell=0}^{3}\Big[\boldsymbol{m}_\ell[k] + \boldsymbol{m}_\ell[k+1]\Big]d_\ell \tag{3.24}$$

Replacing (3.22a) and (3.23) into (3.24), and after some algebraic manipulations, the following expression is obtained:

$$\begin{aligned}\overline{\boldsymbol{x}}_s[k+1] = &\boldsymbol{x}_s[k] + T_s\left(\mathbf{A} + \frac{1}{2}T_0\mathbf{A}^2\right)\boldsymbol{x}_s[k]\sum_{\ell=0}^{3}d_\ell + T_s\mathbf{B}\sum_{\ell=0}^{3}\boldsymbol{u}_{s\ell}d_\ell \\ &+ \frac{1}{2}T_s\left(\mathbf{I} + T_0\mathbf{A}\right)\mathbf{E}\boldsymbol{i}_o[k]\sum_{\ell=0}^{3}d_\ell + \frac{1}{2}T_0\mathbf{A}\mathbf{B}\boldsymbol{u}_j\sum_{\ell=0}^{3}d_\ell + \frac{1}{2}T_s\mathbf{E}\boldsymbol{i}_o[k+1]\sum_{\ell=0}^{3}d_\ell\end{aligned} \tag{3.25}$$

Knowing that $T_0 = T_s/2$ and considering the following:

$$\sum_{\ell=0}^{3}d_\ell = 1 \tag{3.26a}$$

$$\sum_{\ell=0}^{3}\boldsymbol{u}_{s\ell}d_\ell = \boldsymbol{u}_s(d_0 + d_3) + \boldsymbol{u}_{s1}d_1 + \boldsymbol{u}_{s2}d_2 = \boldsymbol{u}_j \tag{3.26b}$$

Expression (3.25) can be simplified as follows:

$$\begin{aligned}\overline{\boldsymbol{x}}_s[k+1] = &\left(\mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2\right)\boldsymbol{x}_s + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}\boldsymbol{u}_j + \frac{1}{2}\left(\mathbf{I} + \frac{1}{2}T_s\mathbf{A}\right)T_s\mathbf{E}\boldsymbol{i}_o[k] \\ &+ \frac{1}{2}T_s\mathbf{E}\boldsymbol{i}_o[k+1]\end{aligned} \tag{3.27}$$

Equation (3.27) is useful when an observer-predictor computes $\boldsymbol{i}_o[k+1]$, and the difference between $\boldsymbol{i}_o[k]$ and $\boldsymbol{i}_o[k+1]$ is sufficiently large. However, if we assume that $\boldsymbol{i}_o[k] \approx \boldsymbol{i}_o[k+1]$ then the average prediction model is simplified to:

$$\overline{\boldsymbol{x}}_s[k+1] = \left(\mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2\right)\boldsymbol{x}_s + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}\boldsymbol{u}_j + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{E}\boldsymbol{i}_o[k] \tag{3.28}$$

Equation (3.28) can be written as the linear representation (3.18) with $\mathbf{A}_d = \mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2$, $\mathbf{B}_d = \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}$, and $\mathbf{E}_d = \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{E}$.

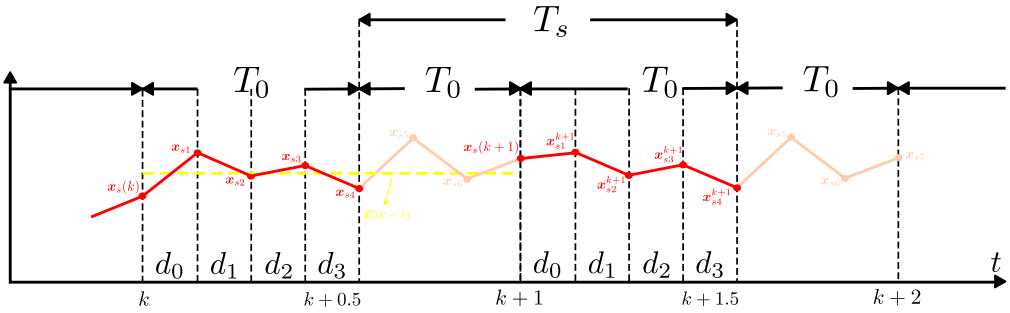


Figure 3.6: Predicted system trajectory using improved Euler's method for a 7S-SS.

3.2. C-OSS-MPC formulation

3.2.1. Reference vector

The objetive of the controllers is to keep the voltage of the LC filter capacitors as sinusoidal waveforms. Thus, the reference voltage vector is

$$\boldsymbol{v}_o^*[k+1] = V^* e^{j\omega t} \tag{3.29}$$

Where V^* is the magnitude of the reference voltage vector, and ω is the fundamental frequency of the output voltage ($\omega = 2\pi f_0$). The reference current is obtained as a function of the reference voltage. Let us plug-in the reference voltage vector into the dynamic equation of the output voltages as

$$\frac{d\boldsymbol{v}_o^*}{dt} = \frac{1}{C_f}\left(\boldsymbol{i}_s^* - \boldsymbol{i}_o\right) \tag{3.30}$$

Solving the equation for $\boldsymbol{i}_s^*$ we obtain

$$\boldsymbol{i}_s^* = \omega C_f \mathbf{J} \boldsymbol{v}_o^* + \boldsymbol{i}_o \tag{3.31}$$

where the matrix $\mathbf{J}$ is defined as

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{3.32}$$

We would like to constrain the reference current to a maximum value, I_{max}. When the amplitude of the reference current is less than the specified limit, the reference current vector is described by eq. (3.31). In the other case, the reference current vector is saturated at I_{max}. Therefore, the constrained reference current is represented by the following piece-wise function:

$$\boldsymbol{i}_s^* = \begin{cases} \omega C_f \mathbf{J} \boldsymbol{v}_o^* + \boldsymbol{i}_o & \|\boldsymbol{i}_s^*\|_2 < I_{max} \\ \frac{I_{max}}{\|\boldsymbol{i}_s^*\|_2} \boldsymbol{i}_s^* & \|\boldsymbol{i}_s^*\|_2 \geq I_{max} \end{cases} \tag{3.33}$$

Thus, the reference state vector is

$$\boldsymbol{x}_s^*[k+1] = \begin{bmatrix} \boldsymbol{i}_s^* \\ \boldsymbol{v}_o^* \end{bmatrix} \tag{3.34}$$

3.2.2. Cost function

At the heart of the MPC strategy lies the cost function. In the cost function, the variables related to the control objectives are weighted to choose the best possible action. In FCS-MPC schemes, the cost function is most commonly designed to minimize the tracking error [78]. However, it has been proven that FCS-MPC strategies without penalization of the control effort are equivalent to quantized dead-beat controllers [48]. Deadbeat controller feature fast dynamic response [86]. However, they have poor robustness against model mismatches, parameter uncertainties, and noise on measured variables [23]. To reduce the issues related to deadbeat controllers, the control effort should be penalized in the cost function (cf. [86]). In this thesis, the outer MPC loop has two objectives: minimize the tracking error between the state vector and its reference, and penalize the control effort. Therefore, the following cost function is defined:

$$J(\boldsymbol{U}_j, \boldsymbol{d}_j) = \|\boldsymbol{x}_s[k+1] - \boldsymbol{x}_s^*[k+1]\|_{\mathbf{Q}}^2 + \lambda_u \|\boldsymbol{u}[k+1] - \boldsymbol{u}_{ss}\|_2^2 \tag{3.35}$$

The positive-definite matrix $\mathbf{Q} = \text{diag}(\lambda_i,\lambda_i,\lambda_v,\lambda_v)$ is used to trade-off the control objectives of the state vector tracking. In a similar manner, the weighting factor λ_u is used to penalize the control effort. The optimization variable of the problem is the average switching vector, $\boldsymbol{u}(k)$. The average switching vector is the product between the switching matrix and duty cycle vector as $\boldsymbol{u}(k) = \boldsymbol{U}\boldsymbol{d}$.

First, the term of the cost function used to penalize the reference tracking error will be reformulated as a function of the average switching vector $\boldsymbol{u}(k)$. If we replace (3.18) in (3.35), we obtain the following:

$$\|\mathbf{A}_d\boldsymbol{x}_s + \mathbf{B}_d\boldsymbol{u} + \mathbf{E}_d\boldsymbol{i}_o - \boldsymbol{x}_s^*[k+1]\|_{\mathbf{Q}}^2 = \|\mathbf{B}_d\boldsymbol{u} - (\boldsymbol{x}_s^*[k+1] - \mathbf{A}_d\boldsymbol{x}_s - \mathbf{E}_d\boldsymbol{i}_o)\|_{\mathbf{Q}}^2 \tag{3.36}$$

If we define $(\boldsymbol{u}'_{db} = \boldsymbol{x}_s^*[k+1] - \mathbf{A}_d\boldsymbol{x}_s - \mathbf{E}_d\boldsymbol{i}_o)$, then:

$$\|\mathbf{B}_d\boldsymbol{u} - \boldsymbol{u}'_{db}\|_{\mathbf{Q}}^2 \tag{3.37}$$

The second term of the cost function in eq. (3.35) has the vector $\boldsymbol{u}_{ss}$. Vector $\boldsymbol{u}_{ss}$ is the steady-state control action. The steady-state control action is the input vector needed to drive the system towards the steady-state solution. The expression for this vector is obtained solving the circuit of Fig. 3.7 for $\boldsymbol{u}_{ss}$. The steady-state control input $\boldsymbol{u}_{ss}$ is defined as:

$$\boldsymbol{u}_{ss} = \frac{2}{V_{dc}} \left\{ \left[\left(1 - \omega^2 L_f C_f\right) \mathbf{I}_2 + (\omega R_f C_f)\, \mathbf{J} \right] \boldsymbol{v}_o^* + \left[R_f \mathbf{I}_2 + \omega L_f \mathbf{J} \right] \boldsymbol{i}_o \right\} \tag{3.38}$$

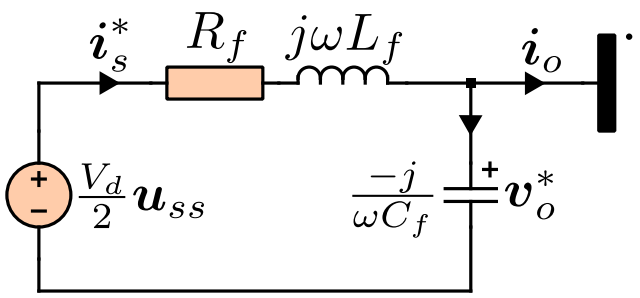


Figure 3.7: Schematic for the steady-state control action.

3.2.3. Optimization problem

In OSS-MPC, the optimal switching sequence (OSS) is obtained solving an optimization problem. The solution must comply with constraints such that the sum of leg duty cycles is equal to one, and each duty cycle must be equal or greater than zero. The optimization problem to solve is the following:

$$\{\boldsymbol{U}^\star, \boldsymbol{d}^\star\} = \arg\min_{\boldsymbol{U}_j} \left\{ \min_{\boldsymbol{d}_j} J(\boldsymbol{d}_j) = \|\mathbf{B}_d \boldsymbol{u}_j(k) - \boldsymbol{u}'_{db}\|^2_{\mathbf{Q}'} + \lambda_u \|\boldsymbol{u}_j(k) - \boldsymbol{u}_{ss}\|_2^2 \right\} \tag{3.39a}$$

$$\text{s.t.} \quad \mathbb{1}^\intercal \boldsymbol{d} = 1 \tag{3.39b}$$

$$\boldsymbol{d}_j \geq \mathbf{0} \tag{3.39c}$$

The optimization problem has the same form as the one solved in [62]. Therefore, the same optimizer will be used. Thus, the usual strategy to solve MPC problems with 3L-NPC converters of evaluating each region $\mathcal{R}_j \in \{\mathcal{R}_1, \ldots, \mathcal{R}_{24}\}$ of the Space of Vectors is avoided.

3.3. Relaxed solution

In this section, the relaxed optimization problem will be solved. The solution of the relaxed optimization problem is the optimal average switching vector (OASV) to be applied during the next sampling instant. Following the principles of Space Vector Modulation, the OASV is synthesized by a sequence of switching vectors. Two cases of the problem are distinguished; First, the linear modulation stage where the duty cycles are positive. Second, the overmodulation stage where the duty cycle of the small switching vectors becomes negative.

3.3.1. Non-negative duty cycles: the linear modulation stage

3.3.1.1. Relaxed optimization problem

To relax the optimization problem, the inequality constraints are removed from the problem formulation. The relaxed optimization problem is then stated as

$$\min_{\boldsymbol{d}} \quad J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) \tag{3.40a}$$

$$\text{s. t.} \quad \mathbb{1}^\intercal \boldsymbol{d} = 1 \tag{3.40b}$$

Lets begin expanding the cost function

$$J_j = (\mathbf{B}_d \boldsymbol{u} - \boldsymbol{u}_{db})^\intercal \boldsymbol{Q} (\mathbf{B}_d \boldsymbol{u} - \boldsymbol{u}_{db}) + \lambda_u (\boldsymbol{u} - \boldsymbol{u}_{ss})^\intercal (\boldsymbol{u} - \boldsymbol{u}_{ss}) \tag{3.41}$$

We get to the following expression

$$\begin{aligned} J_j = \boldsymbol{u}^\intercal (\boldsymbol{Q\prime} + \lambda_u \mathbf{I}_2) \boldsymbol{u} - 2\boldsymbol{u}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}) \\ \ldots + \left(\lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss} + \boldsymbol{u}_{db}'^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db}\right) \end{aligned} \tag{3.42}$$

where $Q\prime$ is the modified weight matrix, $Q\prime = \mathbf{B}_d^\intercal \mathbf{Q} \mathbf{B}_d$. The elements of the switching matrix $\boldsymbol{U}_j \in \mathbb{R}^{2\times 3}$ are the vectors of the switching sequence

$$\boldsymbol{U}_j = \begin{bmatrix} u_{s\alpha} & u_{1\alpha} & u_{2\alpha} \\ u_{s\beta} & u_{1\beta} & u_{2\beta} \end{bmatrix} \tag{3.43}$$

3.3.1.2. Solution of the relaxed optimization problem

Consider the equality constraint of the relaxed optimization problem. We can write the duty cycles for the small switching vectors as a function of the remaining duty cycles.

$$d_{Sj} = 1 - d_{1j} - d_{2j} \tag{3.44}$$

Lets define an auxiliar variable, $\boldsymbol{d}_{\ell j}$, to eliminate the depedent variable d_S from the optimization vector $\boldsymbol{d}_j$:

$$\boldsymbol{d}_{\ell j} = \begin{bmatrix} d_{1j} & d_{2j} \end{bmatrix}^\intercal \tag{3.45}$$

The relationship between $\boldsymbol{d}_j$ and $\boldsymbol{d}_{\ell j}$ is the following

$$\boldsymbol{d}_j = \underbrace{\begin{bmatrix} -1 & -1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}}_{\boldsymbol{M}} \boldsymbol{d}_{\ell j} + \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{N}} \tag{3.46}$$

Then, $\boldsymbol{u} = \boldsymbol{U}\boldsymbol{d} = \boldsymbol{U}(\boldsymbol{M}\boldsymbol{d}_{\ell j} + \boldsymbol{N}) = \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\ell j} + \boldsymbol{U}\boldsymbol{N}$ and $\boldsymbol{u}^\intercal = \boldsymbol{d}^\intercal \boldsymbol{U}^\intercal = (\boldsymbol{M}\boldsymbol{d}_{\ell j} + \boldsymbol{N})^\intercal \boldsymbol{U}^\intercal = \left(\boldsymbol{d}_{\ell j}^\intercal \boldsymbol{M}^\intercal + \boldsymbol{N}^\intercal\right) \boldsymbol{U}^\intercal$. The cost function in terms of $\boldsymbol{d}_{\ell j}$ is

$$\begin{aligned} J = \boldsymbol{d}_{\ell j}^\intercal \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\ell j} + 2\boldsymbol{d}_{\ell j} \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \\ - 2\boldsymbol{d}_{\ell j} \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}) + \boldsymbol{N}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \\ - 2\boldsymbol{N}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}) + \left(\boldsymbol{u}_{db}'^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss}\right) \end{aligned} \tag{3.47}$$

Compute the gradient of J with respect to $\boldsymbol{d}_{\ell j}$ and make it equal to zero

$$\begin{aligned} \nabla J(\boldsymbol{d}_{\ell j}) = \boldsymbol{2}\boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\ell j} + 2\boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \\ - 2\boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}) = \boldsymbol{0} \end{aligned} \tag{3.48}$$

Reorganizing (3.48) to leave the terms related to the duty cycles on the left, (3.49) is obtained

$$\boldsymbol{M}^{\intercal}\boldsymbol{U}^{\intercal}\left(\boldsymbol{Q\prime}+\lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\ell j}=\boldsymbol{M}^{\intercal}\boldsymbol{U}^{\intercal}\left(\mathbf{B}_d^{\intercal}\boldsymbol{Q}\boldsymbol{u}'_{db}+\lambda_u\boldsymbol{u}_{ss}\right)-\boldsymbol{M}^{\intercal}\boldsymbol{U}^{\intercal}\left(\boldsymbol{Q\prime}+\lambda_u\boldsymbol{I}_2\right)\boldsymbol{U}\boldsymbol{N} \quad (3.49)$$

Solving the equation for $\boldsymbol{d}_{\ell j}$ we get

$$\boldsymbol{d}_{\ell j}=\left[\boldsymbol{U}\boldsymbol{M}\right]^{-1}\boldsymbol{u}_{unc}-\left[\boldsymbol{U}\boldsymbol{M}\right]^{-1}\boldsymbol{U}\boldsymbol{N} \quad (3.50)$$

The unconstrained control action ($\boldsymbol{u}_{uc}$) is defined as:

$$\boldsymbol{u}_{uc}=\left(\boldsymbol{Q\prime}+\lambda_u\boldsymbol{I}_2\right)^{-1}\left(\boldsymbol{B}_d^{\intercal}\boldsymbol{Q}\boldsymbol{u}'_{db}+\lambda_u\boldsymbol{u}_{ss}\right) \quad (3.51)$$

Now we need to map the solution back to its original variables. Lets plug-in (3.50) in (3.46), we get

$$\boldsymbol{d}_{rj}=\begin{bmatrix}\boldsymbol{M}\left(\boldsymbol{U}\boldsymbol{M}\right)^{-1} & \boldsymbol{N}-\boldsymbol{M}\left(\boldsymbol{U}\boldsymbol{M}\right)^{-1}\boldsymbol{U}\boldsymbol{N}\end{bmatrix}\begin{bmatrix}\boldsymbol{u}_{uc}\\1\end{bmatrix} \quad (3.52)$$

The optimal duty cycles for the linear modulation stage are computed using the (3×3) matrix

$$\boldsymbol{d}_{rj}=\frac{1}{\Delta}\begin{bmatrix}u_{1\beta}-u_{2\beta} & u_{2\alpha}-u_{1\alpha} & \boldsymbol{u}_1\times\boldsymbol{u}_2\\ u_{2\beta}-u_{s\beta} & u_{s\alpha}-u_{2\alpha} & \boldsymbol{u}_2\times\boldsymbol{u}_s\\ u_{s\beta}-u_{1\beta} & u_{1\alpha}-u_{s\alpha} & \boldsymbol{u}_s\times\boldsymbol{u}_1\end{bmatrix}\begin{bmatrix}u_{uc,\alpha}\\u_{uc,\beta}\\1\end{bmatrix} \quad (3.53)$$

Δ is the determinant of matrix product $\left(\boldsymbol{U}\boldsymbol{M}\right)^{-1}$

$$\Delta=\boldsymbol{u}_S\times\boldsymbol{u}_1+\boldsymbol{u}_2\times\boldsymbol{u}_S+\boldsymbol{u}_1\times\boldsymbol{u}_2 \quad (3.54)$$

Where $\boldsymbol{u}_x\times\boldsymbol{u}_y=u_{x\alpha}u_{y\beta}-u_{x\beta}u_{y\alpha}$ denotes the cross product.

3.4. Optimal Solution

In the previous section, the relaxed solution to the optimization problem was found. The relaxed duty cycles vector $\boldsymbol{d}_{rj}$ is the local solution for each region $j\in\mathcal{R}$ of the control hexagon $\mathbb{V}$. The relaxed solution computed with (3.40) fulfills the equality constraint $\mathbb{1}^{\intercal}\boldsymbol{d}=1$. Thus, all regions can be mapped onto $\boldsymbol{u}_{uc}$ in the $\alpha\beta$-plane. However, only one region fulfills the non-negativity constraint (cf. [53]). The non-negativity constraint can then be considered in the solution with a simple methodology, as in [62, 53, 55]. The metholodogy introduced therein also reduces the computational burden avoiding the search over all 24 regions of the control region $\mathbb{V}$ to only four. The methodology will be explained in this section.

3.4.1. Direct Solution

Lets assume that the unconstrained control action $\boldsymbol{u}_{uc}$ falls inside the control region $\mathbb{V}$, see $\boldsymbol{u}_{uc}^{(1)}$ in Fig. 3.8(b). There exist only one region $\mathcal{R}^{\star}$ whose convex combination of switching vector and duty cycles can synthesize $\boldsymbol{u}_{uc}$. The optimal region $\mathcal{R}^{\star}$ is the one in which the unconstrained control action falls and, at the same time, the only one where the non-negativity constraint $\boldsymbol{d}_{rj}\geq\boldsymbol{0}$ is fulfilled. The vectors who form $\mathcal{R}_1$ in sector 1 are $\boldsymbol{u}_{s1}^{-}$, $\boldsymbol{u}_{s2}^{-}$ and $\boldsymbol{u}_0$. The

switching sequence applied is:

$$\boldsymbol{S} = \left\{ \underbrace{\begin{bmatrix} 0 \\ -1 \\ -1 \end{bmatrix}}_{\boldsymbol{u}_{s1}^-}, \underbrace{\begin{bmatrix} 0 \\ 0 \\ -1 \end{bmatrix}}_{\boldsymbol{u}_{s2}^-}, \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{u}_0}, \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{u}_{s1}^+} \right\} \tag{3.55}$$

Using the three first vectors as $\boldsymbol{u}_s = \boldsymbol{u}_{s1}^-$, $\boldsymbol{u}_1 = \boldsymbol{u}_{s2}^-$, $\boldsymbol{u}_2 = \boldsymbol{u}_0$, and replacing them in (3.53), the duty cycles for $\mathcal{R}_1$ can be found as:

$$\begin{bmatrix} d_{rS} \\ d_{r1} \\ d_{r2} \end{bmatrix} = \begin{bmatrix} \frac{3}{2} & \frac{-\sqrt{3}}{2} & 0 \\ 0 & \sqrt{3} & 0 \\ \frac{-3}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} u_{unc,\alpha} \\ u_{unc,\beta} \\ 1 \end{bmatrix} \tag{3.56}$$

Assume $\boldsymbol{u}_{uc}^{(1)} = m\begin{bmatrix}\cos(\theta) & \sin(\theta)\end{bmatrix}^\intercal$. If $m = 0.4$ and $\theta = \pi/6$, then the duty cycles are $\boldsymbol{d}_{rj} = \begin{bmatrix}\sqrt{3}/5 & \sqrt{3}/5 & 1-(2\sqrt{3})/5\end{bmatrix}^\intercal$. Notice that these duty cycles fulfill both conditions: $\boldsymbol{d}_{rj} \geq 0$ and $\mathbb{1}^\intercal \boldsymbol{d}_{rj} = 1$. However, if $m = 1$ (making $\boldsymbol{u}_{uc}^{(1)}$ fall in $\mathcal{R}_2$) then $\boldsymbol{d}_{rj} = \begin{bmatrix}\sqrt{3}/2 & \sqrt{3}/2 & 1-\sqrt{3}\end{bmatrix}^\intercal$, which do not fulfill the non-negativy constraint.

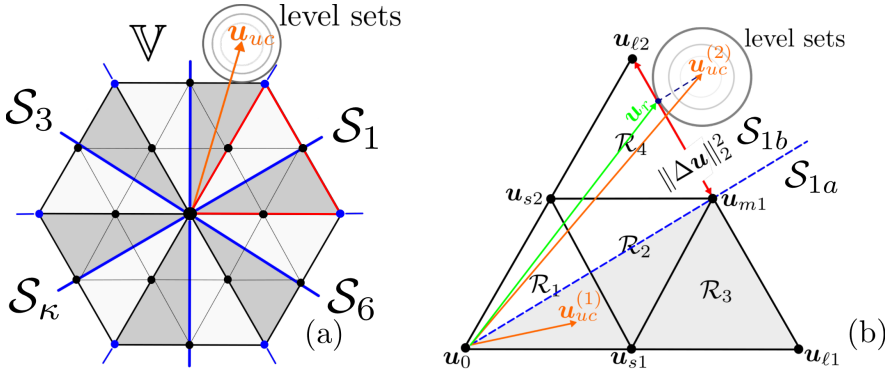


Figure 3.8: Control region of the 3L-NPC. (a) Hexagon divided in 6 sectors to reduce the computational burden of the OSS-MPC algorithm, and (b) close-up look into sectors $\mathcal{S}_{1a}$-$\mathcal{S}_{1b}$.

If the $\alpha\beta$-plane is divided in 6 sectors $\mathcal{S}_\kappa$ where $\kappa \in \{1, \ldots, 6\}$, see Fig. 3.8(a), then the optimal solution must be in one of the four regions inside sector $\mathcal{S}_\kappa$. The optimal sector is found evaluating (3.53) with the switching vectors forming the frontier of the hexagon. The optimal sector is the one where $\boldsymbol{d}_{rj} \geq 0$ and $\mathbb{1}^\intercal \boldsymbol{d}_{rj} = 1$ and fulfulled simultaneously. Consider $\mathcal{S}_1$ (red triangle in Fig. 3.8(a)). The switching vectors forming the frontier are $\boldsymbol{u}_{\ell 1}$, $\boldsymbol{u}_{\ell 2}$, and $\boldsymbol{u}_0$:

$$\boldsymbol{S} = \left\{ \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{u}_0}, \underbrace{\begin{bmatrix} 1 \\ -1 \\ -1 \end{bmatrix}}_{\boldsymbol{u}_{\ell 1}}, \underbrace{\begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix}}_{\boldsymbol{u}_{\ell 2}} \right\} \tag{3.57}$$

Using the vectors in (3.57), the duty cycles for $\mathcal{S}_1$ can be found as:

$$\begin{bmatrix} d_{rS} \\ d_{r1} \\ d_{r2} \end{bmatrix} = \begin{bmatrix} -\frac{3}{4} & \frac{-\sqrt{3}}{4} & 1 \\ \frac{3}{4} & \frac{-\sqrt{3}}{4} & 0 \\ 0 & \frac{\sqrt{3}}{2} & 0 \end{bmatrix} \begin{bmatrix} m\cos(\theta) \\ m\sin(\theta) \\ 1 \end{bmatrix} \tag{3.58}$$

If $m = 0.4$ and $\theta = \pi/6$, then the duty cycles are $\boldsymbol{d}_{rj} = \begin{bmatrix} 1 - (\sqrt{3}/5) & \sqrt{3}/10 & \sqrt{3}/10 \end{bmatrix}^\intercal$. These duty cycles fulfill both conditions: $\boldsymbol{d}_{rj} \geq 0$ and $\mathbb{1}^\intercal \boldsymbol{d}_{rj} = 1$. However, if $m = 2$ (making $\boldsymbol{u}_{uc}^{(1)}$ fall outside the hexagon) then $\boldsymbol{d}_{rj} = \begin{bmatrix} 1 - \sqrt{3} & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix}^\intercal$. The duty cycle of the small vector becomes negative when $\boldsymbol{u}_{uc}$ is outside the hexagon. Finally, if $m = 1$ and $\theta = 2\pi/3$ then $\boldsymbol{d}_{rj} = \begin{bmatrix} 1 & -3/4 & 3/4 \end{bmatrix}^\intercal$. The duty cycle d_{r1} has become negative when $\boldsymbol{u}_{uc}$ is outside the sector defined by the vectors of the frontier.

When $\mathcal{S}^\star$ has been found, the next step is to determine the subsector $\mathcal{S}_a^\star$ or $\mathcal{S}_b^\star$ where $\boldsymbol{u}_{uc}$ is located (see Fig. 3.8(b)). First, compute the angular position (θ_{op}):

$$\theta_{op} = \tan^{-1}\left(\frac{u_{c\beta}}{u_{c\alpha}}\right) - \frac{\pi}{3}\left(\mathcal{S}^\star - 1\right) \tag{3.59}$$

The subsector is found following this simple rule: if $\theta_{op} \leq \pi/6$, then $\boldsymbol{u}_{uc}$ is located in subsector $\mathcal{S}_a^\star$. However, if $\theta_{op} > \pi/6$, then $\boldsymbol{u}_{uc}$ is located in subsector $\mathcal{S}_b^\star$.

The conventional enumeration algorithm can be reduced to only 3 regions after the sector and subsector have been identified. Each sector has three candidate switching sequences, but only one of them fulfill the non-negativity constraint. Thus, the optimal pair $\{\boldsymbol{U}^\star, \boldsymbol{d}^\star\}$ is found evaluating the non-negativity condition over the duty cycles vector of each candidate region. However, if $\boldsymbol{u}_{uc}$ falls outside the control region $\mathbb{V}$ (e.g., see $\boldsymbol{u}_{uc}^{(2)}$ in Fig. 3.8(b)) then none of the candidate switching sequences fulfill the non-negativity constraint.

The aforementioned case occurs during transient operation. The candidate switching sequence is then reduced to one and is built by the small and large switching vectors belonging to the only outer region that intersects the optimal sector. The case is further analyzed in the next subsection.

3.4.2. Handling the negative duty cycles: the overmodulation stage

3.4.2.1. Relaxed optimization problem

The unconstrained average switching vector goes outside the hexagon, thus the duty cycle for the small switching vector becomes negative. If we set $d_{Sj} = 0$, the optimization variable becomes

$$\boldsymbol{d}_j = \begin{bmatrix} 0 \\ d_{1j} \\ d_{2j} \end{bmatrix} \tag{3.60}$$

Consider the equality constraint

$$\mathbb{1}^\intercal \begin{bmatrix} 0 & d_{1j} & d_{2j} \end{bmatrix} = 1 \tag{3.61}$$

Notice that one of the two optimization variables is dependent. Thus, if we set d_{2j} to be dependent of d_{1j}, we can find an auxiliar vector to reduce the equality constrained optimization

problem into an unconstrained optimization problem

$$\boldsymbol{d}_j = \underbrace{\begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix}}_{\boldsymbol{M\prime}} d_{1j} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}}_{\boldsymbol{N\prime}} \tag{3.62}$$

Then, $\boldsymbol{u} = \boldsymbol{U}\boldsymbol{d} = (\boldsymbol{M\prime}\boldsymbol{d}_j + \boldsymbol{N\prime}) = (\boldsymbol{u}_1 - \boldsymbol{u}_2)\, d_1 + \boldsymbol{u}_2$ and $\boldsymbol{u}^\intercal = \boldsymbol{d}_j^\intercal \boldsymbol{U}^\intercal = (\boldsymbol{M\prime}\boldsymbol{d}_j + \boldsymbol{N\prime})^\intercal \boldsymbol{U}^\intercal = (\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal\, d_1 + \boldsymbol{u}_2^\intercal$. The cost function is

$$\begin{aligned} J = {} & (\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)\, d_1^2 + 2\,(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2 d_1 \\ & - 2\,(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right) d_1 + \boldsymbol{u}_2^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2 - 2\boldsymbol{u}_2^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right) \\ & + \left(\boldsymbol{u}_{db}'^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss}\right) \end{aligned} \tag{3.63}$$

3.4.2.2. Solution of the relaxed optimization problem

The unconstrained optimization problem is solved setting to zero the derivative of the cost function with respect to the optimization variable

$$\begin{aligned} \frac{d}{d(d_{1j})} J = {} & 2\,(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)\, d_1 + 2\,(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2 \\ & - 2\,(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right) = 0 \end{aligned} \tag{3.64}$$

Solving it for d_1 yields

$$d_1 = \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right)}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)} - \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)} \tag{3.65}$$

Considering that the weigthing matrix $\boldsymbol{Q}$ is diagonal then $(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2) = \kappa \boldsymbol{I}_2$ with $\kappa > 0$ and $\kappa \in \mathbb{R}$. Thus,

$$d_1 = \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right)}{\kappa\,(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_1 - \boldsymbol{u}_2)} - \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \boldsymbol{u}_2}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_1 - \boldsymbol{u}_2)} \tag{3.66}$$

Bearing on mind that $\boldsymbol{u}_{uc} = \left(\boldsymbol{Q\prime} + \lambda_u \boldsymbol{I}_2\right)^{-1} \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right) = \kappa^{-1} \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right)$, the optimal duty cycle $d_1^\star$ is

$$d_{1j}^\star = \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_{uc} - \boldsymbol{u}_2)}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_1 - \boldsymbol{u}_2)} \tag{3.67}$$

Notice that the denominator of $d_{1j}^\star$ is the length between a large and medium vector in the hexagon frontier (see Fig. 3.8(b)), thus:

$$\|\Delta \boldsymbol{u}\|_2^2 = (\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_1 - \boldsymbol{u}_2) = \frac{4}{9} \tag{3.68}$$

Then, the optimal solution for the overmodulation stage is:

$$d^{\star}_{Sj} = 0 \tag{3.69a}$$

$$d^{\star}_{1j} = \text{mid}\left\{0, \frac{9}{4}(\boldsymbol{u}_1 - \boldsymbol{u}_2)^{\intercal}(\boldsymbol{u}_{unc} - \boldsymbol{u}_2), 1\right\} \tag{3.69b}$$

$$d^{\star}_{2j} = 1 - d_{1j} \tag{3.69c}$$

3.4.3. Neutral-point voltage balancing scheme

The adequate operation of the 3L-NPC requires the control of the neutral-point voltage. In [55], the optimal switching sequence computed with the outer MPC loop is mapped to three-phase control signals. Then, an optimal zero-sequence control signal is computed and added to the three-phase control signals. The zero-sequence control signal is used to balance the NP-voltage. Finally, the control signals are passed to a single-carrier-based PWM strategy to generate the desired pulse pattern, see Fig. 3.9. The same scheme will be used in this work.

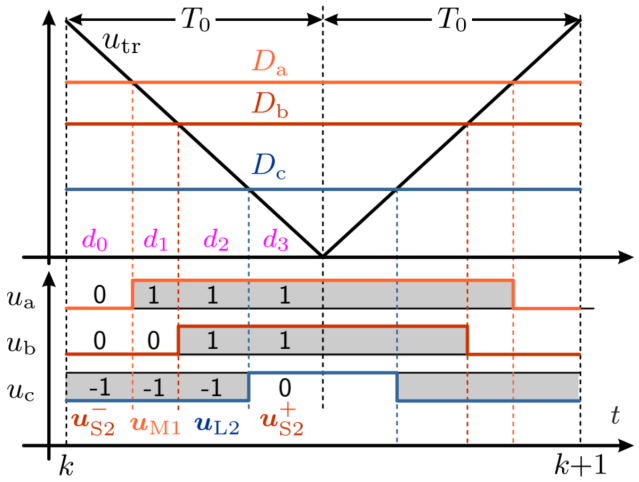


Figure 3.9: Single-carrier PWM strategy for the 3L-NPC (taken from [55]).

First, mapping the optimal switching sequence to three-phase control signals requires a model of the converter. As seen in Fig. 2.1, each leg of the converter is controlled by the variables u_{1x} and u_{2x}, where $x \in \mathcal{P} = \{a, b, c\}$. Variables u_{1x}, $u_{2x} \in \{0, 1\}$ represent the leg gate (or switching) signals. The leg switching state can be represented as a function of the leg gate signals as follows:

$$u_x = u_{1x} + u_{2x} - 1 \tag{3.70}$$

The leg duty cycle can be computed from eq. (3.70). Considering PWM fundamentals, the leg duty cycle is the average value of the leg gate signal over a complete switching cycle (i.e., $D_x = \frac{1}{T_s}\int_0^{T_s} u_x(\tau)d\tau \in [-1, 1]$). Thus, the leg duty cycle is:

$$D_x = D_{1x} + D_{2x} - 1 \tag{3.71}$$

where $D_{1x}, D_{2x} \in [0, 1]$ are the device duty cycles. Considering that the 7S-SS is designed to get just one commutation per leg during one switching cycle and transition between states

+1 and -1 is forbidden, the three-phase control signals for the outer MPC loop are computed as:

$$\boldsymbol{D}_{abc} = d_1^\star \boldsymbol{u}_{abc,1}^\star + d_2^\star \boldsymbol{u}_{abc,2}^\star + \frac{1}{2} d_s^\star \left(\boldsymbol{u}_{abc,0}^\star + \boldsymbol{u}_{abc,3}^\star \right) \tag{3.72}$$

As aforementioned, the three-phase control signal sent to the single-carrier PWM modulator is the sum of the modulating signals computed with eq. (3.72) and an optimal zero-sequence control signal $u_o^\star$. The zero-sequence control signal is the solution to the following optimization problem:

$$u_o^\star = \min_{u_o} \ \left(v_n[k+1] - v_n^* \right)^2 \tag{3.73a}$$

$$\text{s.t.} \quad u_o[k] \in [-\Delta_o, \Delta_o] \tag{3.73b}$$

in which v_n^* is the reference value of the DC-link NP-voltage and Δ_o is a time-varying saturation level introduced in [55] to deal with the nonlinearities of the discrete-time model of the NP-voltage. The discrete-time model of the NP-voltage is obtained using forward Euler's method in eq. (2.4):

$$v_n[k+1] = v_n[k] + \frac{T_s}{C_1 + C_2} \sum_{x \in P} |\underbrace{D_x[k] + u_o[k]}_{D_x^\star}| i_x[k] \tag{3.74}$$

where $D_x^\star$ is the modulating signal that will be passed to the modulator. As mentioned before, To deal with the non-linearity introduced by the absolute value function in eq. (3.74), the common-mode signal is restricted to the set $\mathbb{U}_o \triangleq [-\Delta_o, \Delta_o]$. The time-variying saturation level is defined as:

$$\Delta_o[k] = \min\{1 - |D_x[k]|\} \tag{3.75}$$

Then, the following relationship holds:

$$|D_x[k] + u_o[k]| = \text{sgn}\{D_x[k]\} \left(D_x[k] + u_o[k] \right) \tag{3.76}$$

Substituing eq. (3.76) into (3.74), the NP-voltage discrete-time model can be represented as a linear equation of $u_o[k]$ as follows:

$$v_n[k+1] = v_n[k] + \alpha[k] + \beta[k] u_o[k] \tag{3.77}$$

where $\alpha[k]$ and $\beta[k]$ are determined at eatch sampling instant according to:

$$\begin{aligned} \alpha[k] &= \frac{T_s}{C_1 + C_2} \sum_{x \in \mathcal{P}} |D_x| i_x \\ \beta[k] &= \frac{T_s}{C_1 + C_2} \sum_{x \in \mathcal{P}} \text{sgn}\{D_x\} i_x \end{aligned} \tag{3.78}$$

Thus, the optimal zero-sequence signal to balance the NP-voltage is obtained solving (3.73) as:

$$u_o^\star = \text{mid}\left\{-\Delta_o, -\frac{\alpha[k] - (v_n^* - v_n[k])}{\beta[k]}, \Delta_o\right\} \tag{3.79}$$

The optimal zero-sequence signal is restricted to the set $u_o^\star \in [-0.9\Delta_o, 0.9\Delta_o]$ (cf. [55]). Finally, the three-phase control signals sent to the single-carrier PWM modulator are:

$$\boldsymbol{D}_{abc}^\star = \boldsymbol{D}_{abc} + u_o^\star \tag{3.80}$$

Chapter 4

Simulation and Experimental Results

In this chapter, simulation and experimental results are presented and discussed. This chapter harbors different simulation and experimental tests used to validate the proposed control strategies. A handful of metrics, such as RMS error and total harmonic distortion, are used to compare the performance between the developed controllers. The solution of the proposed algorithm is evaluated against the solver *lsqlin*.

The 3L-NPC converter connected to the LC filter and the proposed C-OSS-MPC strategy were implemented using MATLAB-Simulink® with the PLECS® Blockset package. The plant and load parameters are shown in Table 4.1. The sampling time used for the simulation and experiments is 100 [μs], and the converter switching cycle is 200 [μs].

Table 4.1: System Parameters

Parameter	Value
Sampling frequency f_s	$f_s = 10$ [kHz]
Switching frequency f_c	$f_c = 5$ [kHz]
DC-link voltage	$V_{dc} = 700$ V
LC Filter	$R_f = 1$ mΩ $L_f = 2.4$ mH $C_f = 15$ μF
Load resistance	$R_L = 30$ Ω
Non-linear load	$L_n = 1.8$ mH $C_n = 2.2$ mF $R_n = 460$ Ω

In Fig. 4.1(a), the 3L-NPC with output LC filter is shown. The load phase-to-neutral voltage is measured between the nodes of the capacitor in the filter (i.e., between nodes (a, b, c) and node N). Meanwhile, the converter phase-to-neutral voltages are measured between nodes (u, v, w) at the output of the 3L-NPC and the node between the DC-link capacitors labeled as n. In Fig. 4.1(b), the three-phase resistive load considered is shown. Finally, in Fig. 4.1(c), the nonlinear load is shown. The nonlinear load consist of a three-phase diode rectifier. A 20 [Ω] resistance is placed between the DC output side of the rectifier and the output capacitor to limit the inrush current.

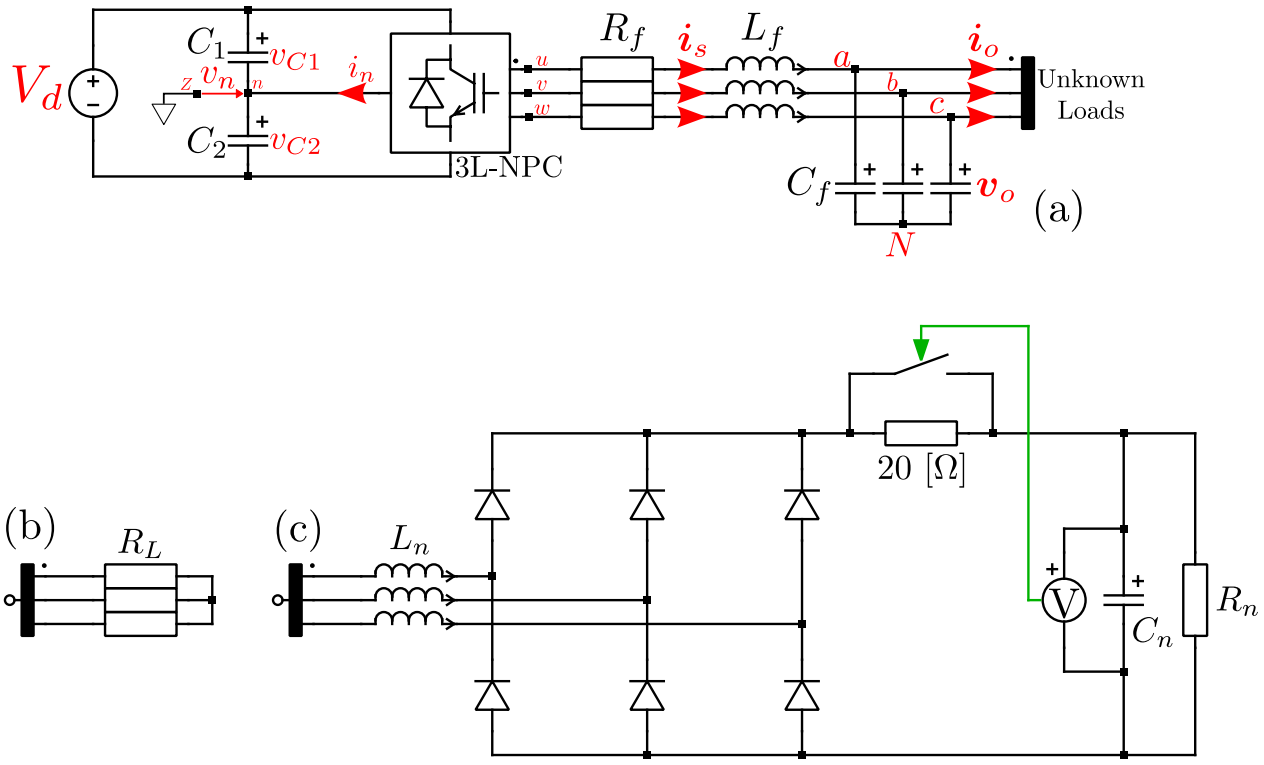


Figure 4.1: System under study. (a) 3L-NPC with output LC filter, (b) Linear resistive load, and (c) Nonlinear load.

4.1. Weighting factors

First, an approach to choose the weigthing factors to compare the performance of the control algorithm with both prediction models is proposed. Remember that the MPC algorithm select a sequence of switching vectors and duty cycles whose linear combination is equal to $\boldsymbol{u}_{uc}$. The expression to compute $\boldsymbol{u}_{uc}$ is:

$$\boldsymbol{u}_{uc} = \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d + \lambda_u \mathbf{I}_2\right)^{-1} \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right) \tag{4.1}$$

In eq. (3.35) the weigthing factor λ_u can be used to trade-off between reference tracking and control effort penalization in the cost function. Then, we would like to use λ_u as a tuning parameter. We can start setting λ_u as:

$$\lambda_u = \mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d \tag{4.2}$$

However, the value of λ_u depends on the paremeters of the discrete matrix $\mathbf{B}_d$ and the weigthing factors in matrix $\boldsymbol{Q}$. Thus, there exist different values of λ_u when forward Euler or improved Euler models are used. To have an unique value of λ_u for both prediction models, the weighting factors λ_i and λ_v have to be chosen appropiately. The expression of $\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d$ for both prediction models is the following:

$$\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d = \left(\frac{V_d T_0}{2 L_f}\right)^2 \lambda_i \tag{4.3a}$$

$$\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d = \left[\frac{V_d T_s}{2L_f}\left(1 - \frac{R_f T_s}{4L_f}\right)\right]^2 \lambda_i + \left[\frac{V_d T_s^2}{8 C_f L_f}\right]^2 \lambda_v \tag{4.3b}$$

where (4.3a) is the expression of $\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d$ for forward Euler model, and (4.3b) is the expression of $\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d$ for improved Euler model. First, notice that (4.3a) does not have the weighting factor λ_v. Thus, we can set $\lambda_v = 0$ in (4.3b). Then, if we set $\lambda_i = 1$ in (4.3a), the expressions (4.3a) and (4.3b) becomes:

$$\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d = \left(\frac{V_d T_0}{2L_f}\right)^2 \tag{4.4a}$$

$$\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d = \left[\frac{V_d T_s}{2L_f}\left(1 - \frac{R_f T_s}{4L_f}\right)\right]^2 \lambda_i \tag{4.4b}$$

Now, we need to find a value for λ_i in (4.4b). The purpose of this operation was to have equal value of λ_u for both prediction models. Then, lets set (4.4a) and (4.4b) equal, and solve for λ_i:

$$\lambda_i = \frac{\left(\frac{T_0}{T_s}\right)^2}{\left(1 - \frac{R_f T_s}{4L_f}\right)^2} \tag{4.5}$$

If we assume $\frac{R_f T_s}{4L_f} \approx 0$, as will be the case in this work, then:

$$\lambda_i = \left(\frac{T_0}{T_s}\right)^2 = \frac{1}{4} \tag{4.6}$$

The weighting factors for matrix $\boldsymbol{Q}$ using forward Euler model or improved Euler model are summarized in Table 4.2:

Table 4.2: Weighting factors for matrix $\boldsymbol{Q}$

Weighting factor	Forward Euler	Improved Euler
λ_i	1	0.25
λ_v	0	0

Then, using the values of Table 4.2, we can get $\lambda_u = \lambda_{u0} = 53.17$ for both prediction models. From this λ_u, we can adjust the performance of the controller incrementing or decreasing its value.

4.2. Performance metrics

The performance of the controllers will be evaluated using the following metrics: RMS error (RMSE), percentual error (E_X), total harmonic distorion (THD), total demand distortion (TDD), settling time, and maximum percent overshoot (M_p) or dip were appropiate. The percentual error is defined as follows:

$$E_X[\,\%] = \frac{100}{\|\boldsymbol{x}^*\|}\sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{P}} \|\boldsymbol{x}(k) - \boldsymbol{x}^*(k)\|_2^2} \tag{4.7}$$

where $\mathcal{P} = \{1, 2, \ldots, N_p\}$ is the set of indices of the measurements vector, and N_p is the total number of elements in the vector. Whenever the desired reference amplitude is unknown, the root-mean-square error (RMSE) will be used. The RMS error is defined as follows:

$$\text{RMSE}(\boldsymbol{x} - \boldsymbol{x}^*) = \sqrt{\frac{1}{N_p} \sum_{k \in \mathcal{P}} \|\boldsymbol{x}(k) - \boldsymbol{x}^*(k)\|_2^2} \tag{4.8}$$

The quality of the waveforms depends on its harmonics content. The harmonics content will be evaluated using the THD and TDD. The THD is defined as follows:

$$\text{THD} = \frac{100}{X_1} \sqrt{\sum_{\substack{h \in \mathbb{N} \\ h>1}} X_h^2} \tag{4.9}$$

where X_1 is the amplitude of the fundamental component. When the fundamental component is low, the THD is high. This could give misleading results in some cases. The TDD may help distinguish those cases where we have high harmonic content or just a small amplitude of the fundamental component. The TDD is defined as follows:

$$\text{TDD} = \frac{100}{X_{nom}} \sqrt{\sum_{\substack{h \in \mathbb{N} \\ h>1}} X_h^2} \tag{4.10}$$

where X_{nom} is the nominal value of the variable evaluated. The nominal values of the system variables are shown in Table 4.3.

Table 4.3: Nominal peak values of system variables

Variable	Nominal value
Load phase-to-neutral voltage	300 [V]
Converter and load current	15 [A]
Converter phase-to-neutral voltage	350 [V]
Converter line-to-line voltage	700 [V]

The transient performance of the controllers will be evaluated using the settling time and maximum percent overshoot (M_p) or voltage drip, as appropiate. The settling time its defined as the time required for the system to settle within a percentage of the input amplitude [84]. Meanwhile, the maximum percent overshoot its the maximum peak value of the response curve measured from the desired (or reference) value (cf. [84]). M_p is computed as follows:

$$\text{M}_p[\,\%] = \frac{c(t_p) - c(\infty)}{c(\infty)} \times 100\,\% \tag{4.11}$$

where $c(t_p)$ is the maximum peak value of the response curve, and $c(\infty)$ is the desired value. Similarly, the voltage drip will be computed when an undervoltage occurs. The drip value will be computed as:

$$\text{Drip}[\,\%] = \frac{c(\infty) - \text{Peak undervoltage}}{c(\infty)} \times 100\,\% \tag{4.12}$$

We want to compare the performance between MPC with discrete model based on forward Euler and improved Euler. The percentual change (P.C.) will be used to compare metrics

between both controllers. Percentual change is used to compare between new and old values, and its defines as follows:

$$\text{Percentual change} = \frac{\text{New value} - \text{Old value}}{|\text{Old value}|} \times 100\,\% \tag{4.13}$$

In MPC schemes is common to use forward Euler discretization to obtain the discrete prediction model. Thus, metrics of forward Euler-based MPC will be regarded as "Old values". By definition, metrics are real positive numbers, therefore we can omit the absolute value in the denominator.

4.3. Simulation results

4.3.1. Evaluation of the solver

The first experiment aims to show how accurate is the solution of the optimization algorithm explained in the previous chapter compared against a commercial solver. In Fig. 4.2, the average optimal switching vector computed by MATLAB solver *lsqlin* and the algorithm proposed by Mora et. al. [53] are compared. Table 4.4 summarize the RMSE error between the average switching vector computed by both solvers. In the first case, Fig. 4.2(a), no load is connected to the LC filter. Both MPC schemes accurately follow the solution given by *lsqlin*. However, the RMSE error of the average switching vector is reduced by 33.61 % when improved Euler's prediction model is used. In the second case, Fig. 4.2(b), a linear resistive load is connected at the output terminals. Similarly, the RMSE error is reduced by 45.71 % when improved Euler's prediction model is used. The third case shown in Fig. 4.2(c) shows when a nonlinear load is connected at the output. In this case, improved Euler's reduces the RMSE error by 37.02 %. Finally, Fig. 4.2(d) shows when the controller operates in the overmodulation range. In all cases, Improved Euler-based MPC achieves a reduction in RMSE error compared with Forward Euler-based MPC. Thus, the solution obtained by the algorithm proposed in [53] with Improved Euler-based prediction model is closer to the solution obtained with MATLAB solver *lsqlin*.

Table 4.4: RMSE error of the average switching vector computed by MATLAB solver and the solver proposed in [53].

RMSE($\boldsymbol{u}_{avg} - \boldsymbol{u}^*_{avg}$)	No load	Linear (resistive) load	Nonlinear load
Forward Euler	0.0119	0.014	0.0181
Improved Euler	0.0079	0.0076	0.0114

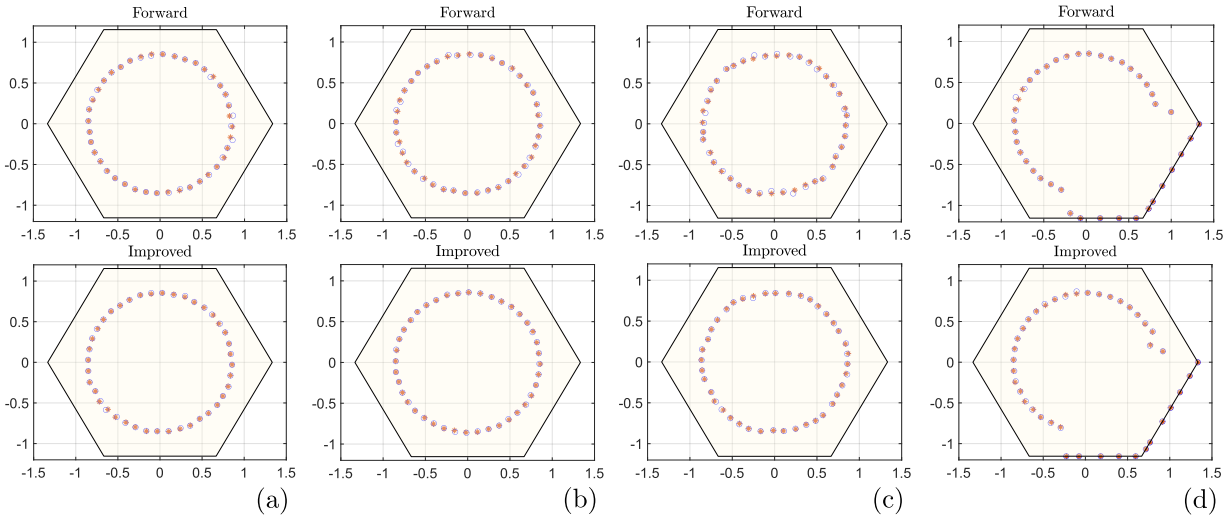


Figure 4.2: Average optimal switching vector computed by MATLAB solver *lsqlin* and the optimization algorithm proposed by Mora et. al. [53]. (a) Forward- and Improved Euler based MPC without load, (b) Forward- and Improved Euler based MPC with resistive load, (c) Forward- and Improved Euler based MPC with nonlinear load, and (d) Forward- and Improved Euler based MPC in the overmodulation region.

4.3.2. Steady-state operation

The second set of simulations explores the performance of the MPC algorithm with forward Euler-based discrete-time model and improved Euler-based discrete-time model. The weighting factor for the control effort is set as $\lambda_u = 212.68$, which is four times bigger than the initial value computed previously (i.e., $\lambda_u = 4\lambda_{u0}$). The unconstrained control action for both models is the following:

$$\boldsymbol{u}_{uc} = \begin{bmatrix} 0.027429 & 0 & 0 & 0 \\ 0 & 0.027429 & 0 & 0 \end{bmatrix} \boldsymbol{u}'_{db} + \begin{bmatrix} 0.8 & 0 \\ 0 & 0.8 \end{bmatrix} \boldsymbol{u}_{uss} \tag{4.14a}$$

$$\boldsymbol{u}_{uc} = \begin{bmatrix} 0.013714 & 0 & 0 & 0 \\ 0 & 0.013714 & 0 & 0 \end{bmatrix} \boldsymbol{u}'_{db} + \begin{bmatrix} 0.8 & 0 \\ 0 & 0.8 \end{bmatrix} \boldsymbol{u}_{uss} \tag{4.14b}$$

where (4.14a) is the control action for forward Euler-based MPC, and (4.14b) is the control action for improved Euler-based MPC.

In Fig. 4.3(a) and Fig. 4.3(c), the load output voltage is shown for forward Euler MPC and improved Euler MPC when the system is operating without load. As can be seen, both methods are capable of accurately track the output voltage reference. However, forward Euler-based MPC presents slightly better performance in this case. The controller based on forward Euler has an RMS voltage error of 3.1 [V], as shown in Fig. 4.3(b). Meanwhile, Fig. 4.3(c) shows that improved Euler-based MPC has an RMS voltage error of 4.07 [V]. Thus, improved Euler MPC increased the average error in 0.32 % with respect to the nominal output voltage of 300 [V]. In Table 4.5, the THD and TDD for the load phase-to-neutral voltage and load line-to-line voltage are shown. Both controllers achieve a small harmonic content in the output voltage. Forward Euler-based MPC has a THD phase-to-neutral load voltage value of 1.58 % and a TDD phase-to-neutral load voltage value of 1.57 %. Meanwhile, improved Euler-based

MPC has a THD phase-to-neutral load voltage value of 2.31 % and a TDD phase-to-neutral load voltage value of 2.30 %. Then, improved Euler-based MPC increased the THD and TDD of the load phase-to-neutral load voltage in 0.73 %. The same values are obtained for the THD and TDD of the line-to-line load voltage.

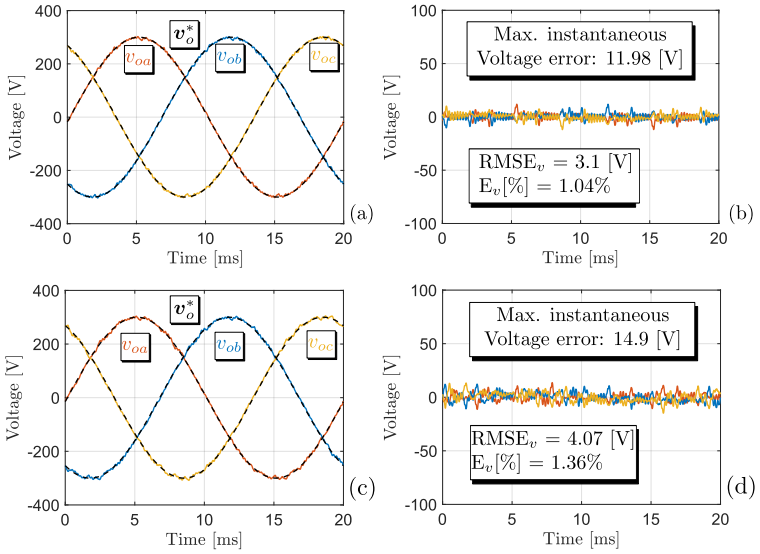


Figure 4.3: Simulation results of the system without load. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

In Fig. 4.4(a) and Fig. 4.4(c), the load output voltage is shown for forward Euler MPC and improved Euler MPC when the system is operating with linear load. In this case, improved Euler-based MPC shows better tracking and harmonic performance. In Fig. 4.4(b), the instantaneous voltage error for forward Euler-based MPC is shown. Forward Euler-based MPC has an RMS voltage error of 2.83 [V]. Meanwhile, improved Euler-based MPC has a RMS voltage error of 0.8 %, as shown in Fig. 4.4(d). Thus, an improvement of 0.14 % is achieved using improved Euler-based MPC with respect to the nominal phase-to-neutral load voltage. In Table 4.5, the THD and TDD for the load voltage and current are shown. The THD and TDD for the load phase-to-neutral voltage using forward Euler-based MPC are 1.62 % and 1.61 %, respectively. The same metrics for improved Euler-based MPC have a value of 1.46 %. Thus, an improvement of 0.12 % in the harmonic content of the load output voltage can be obtained using improved Euler-based MPC. The load current for the MPC algorithm with both models can be seen in Fig. 4.6(a) and Fig. 4.6(b). The load current has better harmonic content using improved Euler-based MPC with an improvement of 0.16 % in its THD and 0.12 % in its TDD.

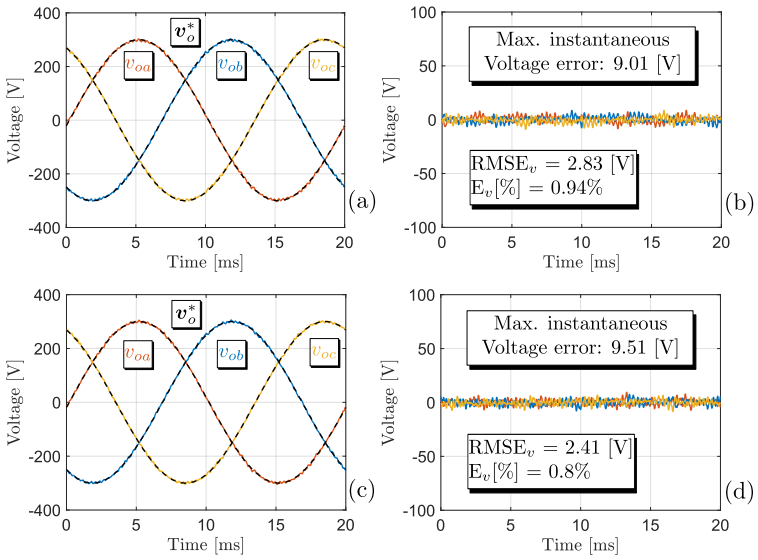


Figure 4.4: Simulation results of the system with linear load. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

The last case analyzed in steady-state is the system operating with a three-phase nonlinear load as shown in Fig. 4.1(c). In Fig. 4.5(a) and Fig. 4.5(c) the load output voltage is shown for forward Euler MPC and improved Euler MPC when the system is operating with a nonlinear load. In this case, the system with forward Euler-based MPC has a better tracking and harmonic performance. The RMS voltage error for forward Euler MPC is 5.5 [V], as shown in Fig. 4.5(b). Meanwhile, the RMS voltage error for improved Euler MPC was 6.62 [V]. Thus, the RMS error increased 0.38 % with respect to the nominal phase-to-neutral load voltage when improved Euler MPC was used. The THD and TDD of the phase-to-neutral load voltage for forward Euler MPC are 2.98 % and 2.97 %, respectively (see Table 4.5). In the case of improved Euler MPC, the same metrics have a value of 3.26 %. Thus, improved Euler MPC increased the THD and TDD of the load voltage in 0.28 %. In Fig. 4.6(c) and Fig. 4.6(d), the load current for the system using both methods is shown. The current drawn by the nonlinear load is highly distorted with a THD of 92.53 % and 90.49 % for forward Euler MPC and improved Euler MPC, respectively. However, even with nonlinear load and a high distortion in the load current, both methods achieved good tracking performance.

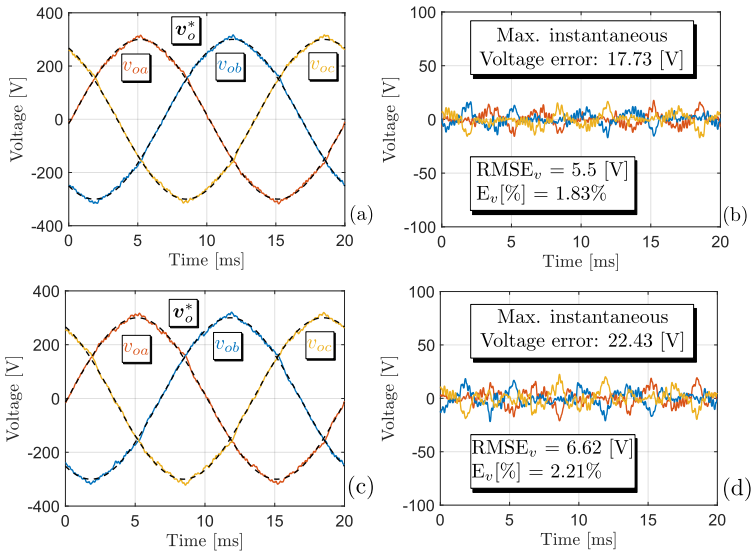


Figure 4.5: Simulation results of the system with nonlinear load. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

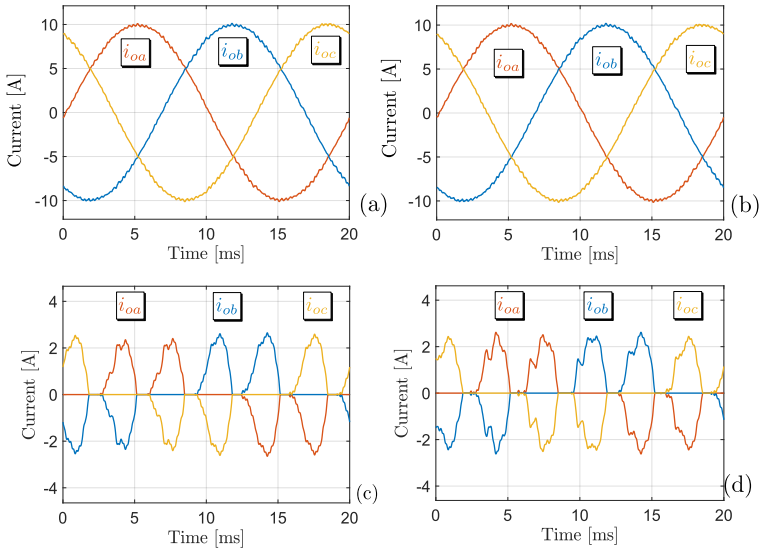


Figure 4.6: Simulation result of the system with linear and nonlinear load. (a) Load current for forward Euler MPC and linear load, (b) Load current for improved Euler MPC and linear load, (c) Load current for forward Euler MPC and nonlinear load, and (d) Load current for improved Euler MPC and nonlinear load.

4.3.3. Performance under reference voltage step

The transient performance of the system when a reference voltage step is applied will be studied. The reference voltage will change from 0 [V] to 300 [V]. In Fig. 4.7(a) and 4.7(b), the

Table 4.5: THD and TDD for load voltage and current in simulation.

Forward Euler-based MPC						
Condition	THD phase-to-neutral Load voltage	TDD phase-to-neutral Load voltage	THD line-to-line Load voltage	TDD line-to-line Load voltage	THD load current	TDD load current
No load	1.58	1.57	1.58	1.57	-	-
Linear load	1.62	1.61	1.62	1.61	1.62	1.1
Nonlinear load	2.98	2.97	2.98	2.97	92.53	7.16
Improved Euler-based MPC						
No load	2.31	2.30	2.31	2.30	-	-
Linear load	1.46	1.46	1.46	1.46	1.46	0.98
Nonlinear load	3.26	3.26	3.26	3.26	90.49	7.12

load voltage in the synchronous reference frame is shown for forward Euler-based MPC and improved Euler-based MPC. As can be seen, forward Euler-based MPC has better dynamic performance than improved Euler-based MPC. The settling time of forward Euler MPC is 0.82 [ms]. Meanwhile, improved Euler-based MPC takes 2.08 [ms] to enter the band around the 300 [V] reference voltage. Thus, the settling time increases in 1.26 [ms] when improved Euler MPC is used. The overshoot of the system increases as well. Forward Euler-based MPC have an $M_p[\,\%]$ of 11.27 %, which means a peak voltage of 333.81 [V]. On the other hand, improved Euler-based MPC have an $M_p[\,\%]$ of 44.42 %, which is a peak voltage of 433.26 [V]. Thus, the maximum percent overshooot increase 33.15 % with improved Euler MPC.

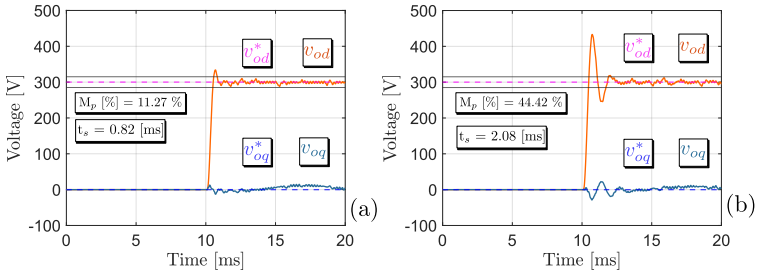


Figure 4.7: Simulation result of the controller with forward and improved Euler model when reference voltage changes from 0 [V] to 300 [V]. (a) Load voltage for forward Euler-based controller, (b) Load voltage for improved Euler-based controller.

4.3.4. Performance under linear resistive load connection

In this section, the transient performance of the system under a linear resistive load connection is studied. The system will be operating with a reference voltage of 300 [V] and without load when a three-phase resistive load of 30 [Ω] per phase is connected. In Fig. 4.8(a) and Fig. 4.8(b), the load voltage for forward Euler-based MPC and improved Euler-based MPC is shown. We can see that improved Euler based have a slightly faster dynamic response at the cost of a increased voltage dip. Forward Euler-based MPC have a settling time of 0.7 [ms]. Meanwhile, improved Euler-based MPC have a settling time of 0.67 [ms]. Thus, improved Euler MPC reach the voltage band 0.03 [ms] faster than forward Euler MPC (the percentual change of the settling time between both methods is 4.48 %). However, the voltage dip of improved Euler MPC is 33.16 % (which means a max. undervoltage of 200.52 [V]). Meanwhile, the voltage dip of forward Euler MPC is 29.66 % which results in a max. undervoltage of 211.02 [V]. Then, improved Euler-based MPC increase the voltage dip in 3.5 % for a 4.47 % improvement in the settling time.

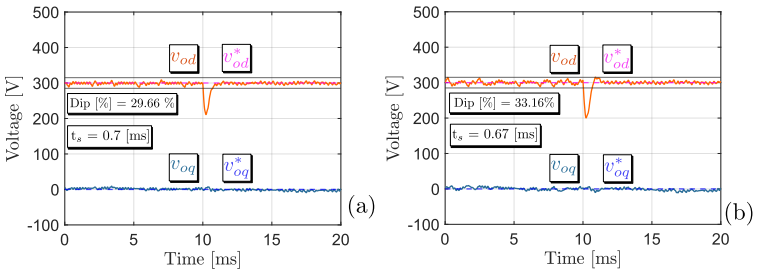


Figure 4.8: Simulation result of the controller with forward and improved Euler model when a linear load is connected. (a) Load voltage for forward Euler-based controller, (b) Load voltage for improved Euler-based controller.

4.4. Experimental results

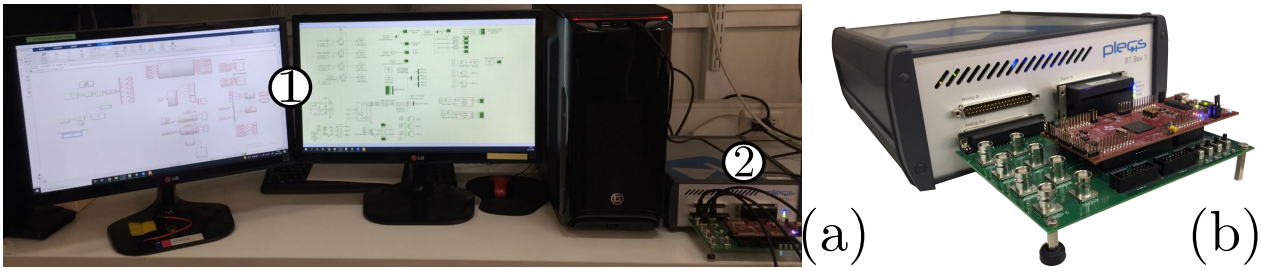


Figure 4.9: Experimental setup used. (a) Host PC and PLECS RT Box 1, and (b) PLECS RT Box 1 with LaunchXL-F28379D mounted over LaunchPad Interface Board.

The experimental results were obtained using PLEXIM Hardware-in-the-Loop (HIL) platform, RT Box 1. Built with a Xilinx Zynq Z-7030 system-on-chip which embeds two CPU cores on an FPGA [87], the RT Box 1 is specifically designed for HIL simulation of power electronics circuits. The platform has 16 analog input/output channels, and 32 digital input/output channels. Thus, it receives the gating signals for the power electronics converter from a microcontroller, and sends the system response through the analog channels.

The control algorithm is executed by Texas Instrument (TI) TMS320F28379D MCU in the LaunchXL-F28379D development kit. The TMS320F28379D is a 32-bit Dual-Core MCU with a 200 MHz clock, 24 single-ended input 12-bit ADC channels (or 12 differential input 16-bit ADC channels), 24 PWM channels, among other peripherals [88]. The LaunXL-F28379D development kit is connected to the RT Box through the RT Box LaunchPad Interface. The LaunchPad Interface facilitates simple connection between TI development kits and the RT Box [89]. A RT Box 1 with a LaunchPad Interface and the LaunchXL-F28379D is shown in Fig. 4.9(b).

In Fig. 4.9(a), the RT Box is connected to a host PC. The plant model and control algorithm are built using PLECS Standalone in the host PC, and then uploaded to the RT Box and MCU. The control algorithm is built using PLECS C-script. Meanwhile, the MCU peripherals are programmed using built-in PLECS blocks. The plant and control algorithm model will be detailed in the appendix A.

4.4.1. Steady-state operation

The first experiment considers the operation of the system without load. In Fig. 4.10(a) and 4.10(b), the load voltage is shown for forward Euler-based MPC and improved Euler-based MPC, respectively. It can be seen that improved Euler-based MPC has a better tracking performance than forward Euler-based MPC. The RMS voltage error for forward Euler MPC is 8.7 [V], as shown in Fig. 4.10(b). Meanwhile, the RMS voltage error of improved Euler MPC is 8.19 [V], as shown in Fig. 4.10(d). Thus, improved Euler MPC improved the average voltage error in 0.17 % with respect to the nominal output voltage of 300 [V] in the experimental setup. In Table 4.6, the THD and TDD for the load phase-to-neutral voltage is shown for both cases. Forward Euler MPC have a THD and TDD for the phase-to-neutral voltage of 3.01 % and 2.95 %, respectively. Meanwhile, improved Euler MPC have have a THD and TDD for the same variable of 3.06 % and 3 %. Thus, forward Euler MPC has an improvement of 0.05 % in the phase-to-neutral load voltage THD and TDD.

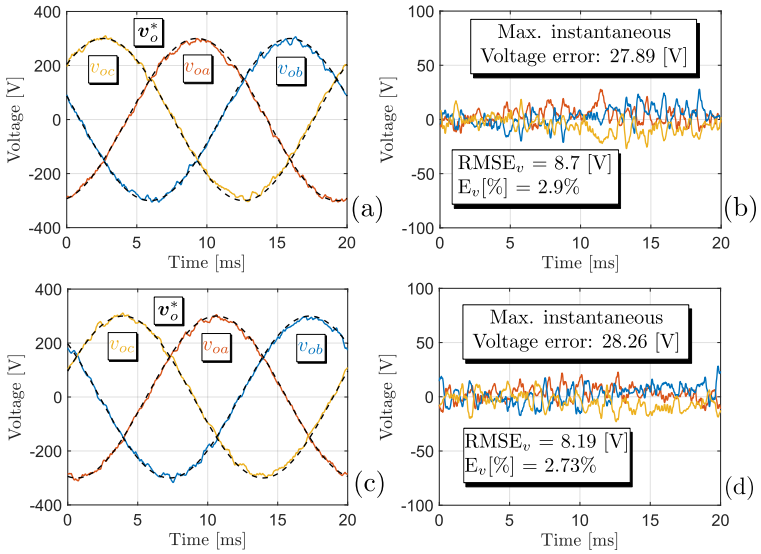


Figure 4.10: Experimental HIL results of the system without load. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

The operation of the system with a linear resistive load is considered. In Fig. 4.11(a) and Fig. 4.11(c), the load voltage for forward Euler MPC and improved Euler MPC is shown. In this case, improved Euler-based MPC have better performance than forward Euler-based MPC. In Fig. 4.11(b), the instantaneous voltage error for forward Euler MPC is shown. For this controller, the RMS voltage error is 7.56 [V]. Meanwhile, the RMS voltage error for improved Euler MPC is 6.2 [V]. Therefore, an improvement of 0.45 % in the average voltage error is obtained with improved Euler MPC. Furthermore, it also has better harmonic performance when a linear load is considered. In Table 4.6, the THD and TDD for the load voltage and current is shown. The THD and TDD for the phase-to-neutral load voltage with forward Euler MPC are 2.03 % and 1.99 %, respectively. In the case of improved Euler MPC, the same variables have a value of 1.56 % and 1.54 %, respectively. Thus, an improvement of 0.47 % and 0.45 % for the THD and TDD of the phase-to-neutral load voltage is obtained

when improved Euler MPC is used. In Fig. 4.13(a) and 4.13(b), the load current for both methods is shown. The THD and TDD of the load current using forward Euler MPC are 2.03 % and 1.32 % respectively. Meanwhile, improved Euler MPC has a value of 1.56 % and 1.02 % for the same variables. Thus, an improvement of 0.47 % and 0.3 % is obtained for the load current THD and TDD when improved Euler is used.

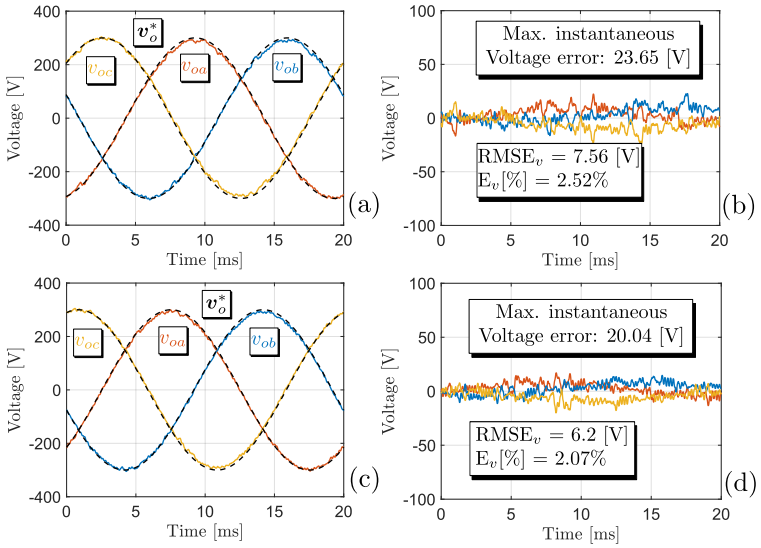


Figure 4.11: Experimental HIL results of the system with linear load. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

The last study case in steady-state operation is the system with a nonlinear load. In Fig. 4.12(a) and Fig. 4.12(c), the load voltage is shown for this case. In this case, forward Euler MPC has a better tracking and harmonic performance than improved Euler MPC. In Fig. 4.12(b), the instantaneous voltage error for forward Euler MPC is shown. The RMS voltage error for this method is 8.68 [V]. Meanwhile, the RMS voltage error for improved Euler MPC is 9.79 [V], as shown in Fig. 4.12(d). Thus, the average voltage error increased in 0.36 % with respect to the nominal load voltage when improved Euler MPC was used. Regarding the harmonic performance of the system, the THD and TDD for the phase-to-neutral load voltage are 2.96 % and 2.90 %, respectively, when forward Euler MPC is used. On the other hand, the THD and TDD for the same variable using improved Euler MPC are 4.11 % and 4.04 %, respectively (see Table 4.6). Thus, the phase-to-neutral THD and TDD increase in 1.15 % when improved Euler MPC is used. The nonlinear load draw a highly distorted current, as shown in Fig. 4.13(c) and Fig. 4.13(d). The THD and TDD of the load current for forward Euler MPC are 70.34 % and 5.41 %. Meanwhile, the THD and TDD of the load current for improved Euler MPC are 93.85 % and 7.79 %. In both cases, the THD is high because the fundamental component of the load current is small (approximately 2.2 [A]).

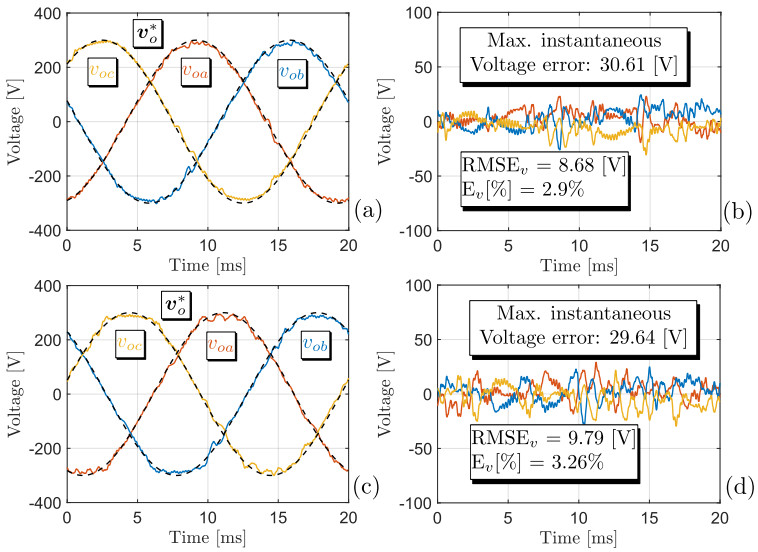


Figure 4.12: Experimental HIL results of the system with nonlinear load. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

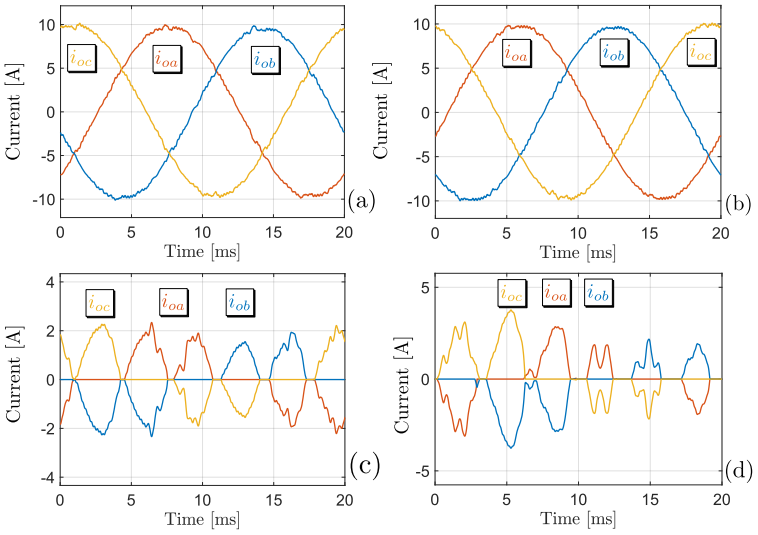


Figure 4.13: Experimental HIL result of the system with linear and nonlinear load. (a) Load current for forward Euler MPC and linear load, (b) Load current for improved Euler MPC and linear load, (c) Load current for forward Euler MPC and nonlinear load, and (d) Load current for improved Euler MPC and nonlinear load.

In Fig. 4.14, the voltage of the capacitors in the DC-link are shown. Only forward Euler-based MPC was selected because the inner MPC is the same for both strategies. The aim is to show that inner MPC reach its goal of balancing the voltage in the DC-link capacitors for the three studied conditions. The worst case is when a linear load is connected. Under that circumstances, $|v_{dc,1} - v_{dc,2}| = 1.49$ $[V]$. This voltage difference is 0.43 % of the desired voltage for the DC-link capacitors which is 350 [V] each. Meanwhile, the voltage difference

in the other conditions of operation is less than 1 [V].

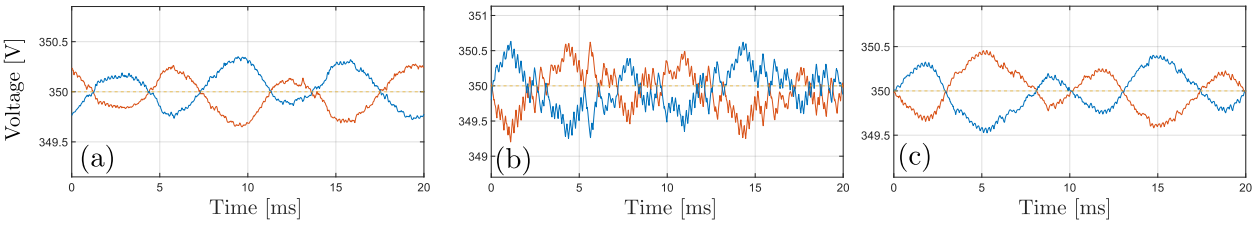


Figure 4.14: DC-link voltages in steady-state operation for forward Euler-based MPC. (a) No load, (b) Linear load, and (c) Nonlinear load.

Table 4.6: THD and TDD of the load voltage and current for forward and improved Euler-based MPC in HIL.

Forward Euler-based MPC						
Conditions	THD phase-to-neutral Load voltage	TDD phase-to-neutral Load voltage	THD line-to-line Load voltage	TDD line-to-line Load voltage	THD load current	TDD load current
No load	3.01	2.95	3.01	2.95	-	-
Linear load	2.03	1.99	2.03	1.99	2.03	1.32
Nonlinear load	2.96	2.90	2.96	2.90	70.34	5.41
Improved Euler-based MPC						
No load	3.06	3.00	3.06	3.00	-	-
Linear load	1.56	1.54	1.56	1.54	1.56	1.02
Nonlinear load	4.11	4.04	4.11	4.04	93.85	7.79

4.4.2. Transient operation

In Fig. 4.15, the transient performance of the system with forward Euler MPC and improved Euler MPC is studied. All the studied changes happen at approximately 4 [ms] ($t \approx 4$ [ms]). It can be seen that forward Euler MPC has a better dynamic performance than improved Euler MPC. In Fig. 4.15(a) and Fig. 4.15(b) the system is operating in steady-state with a reference voltage of 300 [V] when a linear load is connected. When the load is connected, the load voltage drops. Forward Euler MPC takes 0.59 [ms] to recover from the sudden connection of a linear load. Meanwhile, improved Euler MPC takes 0.64 [ms] to recover from the load connection. Thus, improved Euler MPC shows a slower dynamic response in the case of sudden load connection needing 0.05 [ms] to enter the band around the reference voltage value. It also has a 0.49 % larger voltage dip.

In Fig. 4.15(c) and 4.15(d), the transient response of forward Euler MPC and improved Euler MPC is shown for a load disconection. In this case, the system is operating in steady-state with a reference voltage of 300 [V] and feeding a linear resistive load. Suddenly, the load is disconnected from the output terminals of the LC filter. In this case, improved Euler MPC have a faster dynamic performance and a bigger overshoot. When the linear load is disconnected, the load voltage increments. Forward Euler MPC takes only 0.51 [ms] to reduce the voltage overshoot. However, it takes an extra 10.94 [ms] to mitigate the oscillations of the load voltage and enter the band around the reference load voltage. Thus, a settling time of 11.45 [ms] is obtained with forward Euler MPC. On the other hand, improved Euler MPC has a 3.7 % bigger overshoot than forward Euler MPC. However, the load voltage enter the band around the refence voltage after 1.28 [ms].

Finally, the last case studied is a step change in the load reference voltage from 0 [V] to 300 [V]. In Fig. 4.15(e), the load voltage for forward Euler MPC is shown. The settling

time for this case is 2.29 [ms] with an overshoot of 6.23 %. Meanwhile, improved Euler MPC has a settling time of 2.85 [ms] with an overshoot of 36.16 % as shown in Fig. 4.15(f). Thus, forward Euler MPC has a faster transient response during a change of the load reference voltage. Also, notice that improved Euler MPC has an oscillatory response characteristic of second-order systems.

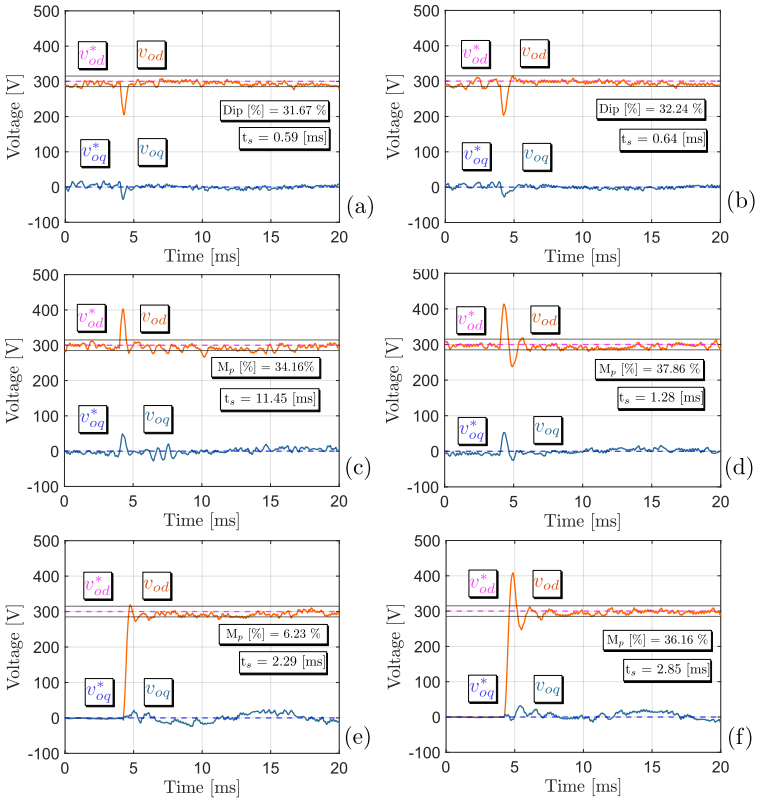


Figure 4.15: Experimental result of the controller during transient operation. (a) Load voltage for forward Euler-based controller during load connection, (b) Load voltage for improved Euler-based controller during load connection, (c) Load voltage for forward Euler-based controller during load disconnection, (d) Load voltage for improved Euler-based controller during load disconnection, (e) Load voltage for forward Euler-based controller during reference voltage step, (f) Load voltage for improved Euler-based controller during reference voltage step.

4.4.3. Discussion of the results

In all the analyzed cases, both forward Euler-based MPC and improved Euler-based MPC were capable of achieving good tracking and harmonics performance. When the steady-state results are considered, improved Euler MPC achieved better performance in two cases: the system operating without load, and the system operating with linear load. The percentual voltage error in both cases were 2.73 % and 2.07 %, respectively. This percentual error is compared with respect to the nominal voltage of 300 [V]. Meanwhile, forward Euler-based MPC achieved better tracking performance when a nonlinear load was connected. In that case, forward Euler got a percentual voltage error of 2.9 % while improved Euler MPC obtained 3.26 %. Furthermore, forward Euler MPC achieved faster dynamic performance than

improved Euler MPC, as seen in Fig. 4.15.

A discrepancy exist between the simulation and experimental results. In simulation, forward Euler-based MPC obtained better tracking performance than improved Euler MPC when the system was operating without load. However, the opposite occured in the experimental results where improved Euler MPC achieved better tracking performance. This is due to a delay of one sampling step in the measurements. To test this hypothesis, the nonideal conditions of implementation were added to the simulation. First, a turn-on delay of 1 $[\mu s]$ and an averaging step of 10 $[\mu s]$ were added to the switching signals of the converter. The turn-on delay was added to simulate the dead-time included in the gating signals generated by the Delfino. Meanwhile, the averaging step was included to simulate the behavior of the PWM Capture block used in the RT Box to read the PWM signals sent by the Delfino (more details about the PWM block can be found in appendix A). However, even with this conditions, forward Euler MPC was able to achieve better tracking performance than improved Euler MPC. Then, a one-step delay of T_s was added to the measured signals in the simulation. In that case, the results shown in Fig. 4.16 were obtained. As can be seen, when the delay is included, improved Euler MPC achieves better tracking performance than forward Euler MPC in the case where the system is operating without load. This is due to the principle behing improved Euler model. In improved Euler model, the predicted value in instant $(k+1)$ is the average slope between the state trajectory during time-intervals $[k, k+1)$ and $[k+1, k+2)$ when a 7S-SS is applied. Thus, the model was capable of compensating the delay in the measurements.

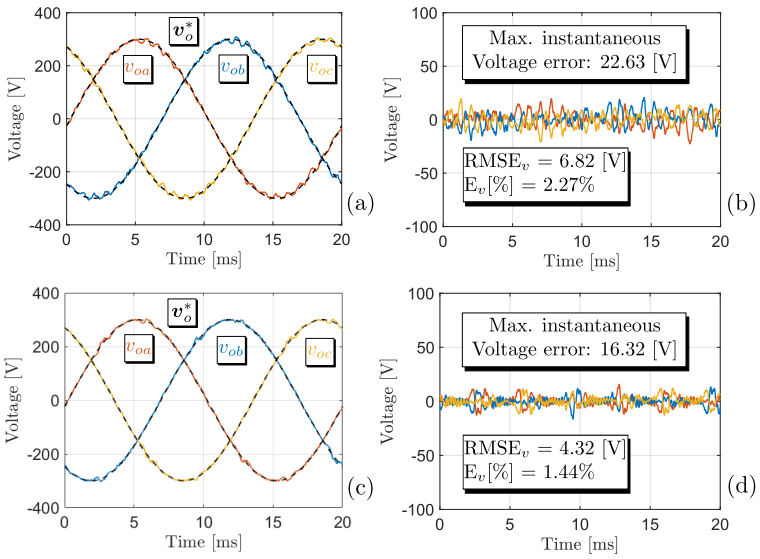


Figure 4.16: Simulation results of the system without load and considering nonideal conditions. (a) Load output voltage for forward Euler MPC, (b) Instantaneous voltage error for forward Euler MPC, (c) Load output voltage for improved Euler MPC, and (d) Instantaneous voltage error for improved Euler MPC.

Another issue is the performance of improved Euler MPC when a nonlinear load is connected. In simulation and experimental results, improved Euler MPC showed worst performance than forward Euler MPC in this case. The reasons are two: (1) the elements of the matrix multiplying $\boldsymbol{u}'_{db}$ in (4.14b) are smaller than those used for forward Euler in (4.14a), and (2)

the value of λ_u is high. When λ_u is high, the system tends towards open-loop operation. Thus, the harmonic components introduced by the nonlinear load have a more significant effect in the performance of the system. This can be seen in appendix B where improved Euler MPC with a value of $\lambda_u = 0$ was considered. When $\lambda_u = 0$, the best THD for the phase-to-neutral load voltage is obtained. However, the THD of the load voltage increased with the value of λ_u.

Regarding the value of the elements in the matrix multiplying $\boldsymbol{u}'_{db}$. In this case, the values of the matrix were smaller for improved Euler MPC. As a consequence, the tracking component of the cost function had less impact over the solution and the unconstrained control action of improved Euler MPC tended more towards the open-loop solution than forward Euler MPC. To solve the issue, a new method to choose the weighting factors must be used. As before, the weight factor for the control effort will be set as $\lambda_u = \mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d$. Then, the unconstrained control action will be:

$$\boldsymbol{u}_{uc} = \frac{1}{2} \left(\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d \right)^{-1} \mathbf{B}_d^\intercal \boldsymbol{Q} \boldsymbol{u}'_{db} + \frac{1}{2} \boldsymbol{u}_{ss} \tag{4.15}$$

Considering $\lambda_u = \mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d$, the matrix multiplying $\boldsymbol{u}_{ss}$ will be the same for both prediction models even when λ_u have different values between forward Euler model and improved Euler model. Then, the problem is to find the values of the weighting factors λ_i and λ_v such that the matrix $\left(\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d \right)^{-1} \mathbf{B}_d^\intercal \boldsymbol{Q}$ multiplying $\boldsymbol{u}'_{db}$ in forward Euler MPC and improved Euler MPC have the same values.

Chapter 5

Conclusion and future work

In this thesis, an Optimal Switching Sequence MPC (OSS-MPC) algorithm was proposed for the three-level neutral-point-clamped (3L-NPC) inverter with output LC filter. The strategy is an extension of the Cascaded Optimal Switching Sequence MPC (C-OSS-MPC) proposed in the literature for current and direct power control of active front-end 3L-NPC inverters.

The control objectives of the algorithm were two: (1) achieve good tracking performance for the converter current and load voltage, and (2) mantain balanced the neutral-point voltage between the DC-link capacitors of the converter. To achieve the objectives, the strategy solves two cascaded optimization problems. The first optimization problem -called outer optimization loop- computes the optimal sequence of switching vectors and their corresponding duty cycles to achieve the objectives related to tracking of the AC side variables. Then, the optimal solution of the outer optimization loop is used by an inner optimization loop to compute an optimal zero-sequence signal designed to balance the neutral-point voltage between the DC-link capacitors.

In this work, two discrete-time models were used to predict the future values of the state vector trajectory. The first model is based on forward Euler discretization. This discretization method is commonly used for power electronics applications. The second model is based on improved Euler discretization. At the best of the author knowledge, improved Euler discretization has not been used in MPC for power electronics converters. Thus, a general discrete-time model considering a linear system in state-space form was derived. The model assumes that a 7S-SS is applied to the converter.

The weighting factors of the cost fuction were choosen to compare the control algorithm with forward Euler model and improved Euler model. First, the weight factor to penalize the control effort of the converter was set to $\lambda_u = \mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d$. However, λ_u had different values for forward Euler-based MPC and improved Euler-based MPC. Thus, the weighting factors λ_i and λ_v related to reference tracking were chosen to make λ_u equal in both models. This method has the following flaw: the solution using improved Euler-based MPC has a stronger tendency towards open-loop solution than forward Euler-based MPC.

Simulation and experimental results are provided to validate the performance of the proposed strategy. Simulations were carried out using MATLAB-Simulink® with the PLECS® Blockset package. Meanwhile, experimental results were obtained using PLEXIM Hardware-in-the-Loop (HIL) platform RT Box 1 to emulate the power electronics stage, and the control algorithm was executed by Texas Instrument (TI) TMS320F28379D MCU in the LaunchXL-

F28379D development kit.

Three cases were considered in steady-state operation: (1) system performance without load, (2) system performance with linear load, and (3) system performance with nonlinear load. In all cases, the MPC algorithm with forward Euler discrete-time model and improved Euler discrete-time model was capable of achieving good tracking performance with low harmonic content in the load voltage. Forward Euler-based MPC showed better performance than improved Euler-based MPC during simulation, when ideal conditions for the system were considered. However, improved Euler-based MPC showed better performance when nonideal conditions -such as a delay in the measured variables- were present. The only case were forward Euler-based MPC achieves better performance in the presence of nonideal conditions is when a nonlinear load is considered. In that case, forward Euler-based MPC achieves 0.36 % less RMS voltage error than improved Euler-based MPC. This result could be due to a poor selection of the weighting factors related to tracking components of the cost function for improved Euler.

The transient performance of the system was studied for three cases: (1) sudden connection of a linear resistive load to the system when it is operating in steady-state with a reference voltage of 300 [V], (2) sudden disconnection of a linear resistive load when the system is operating in steady-state with a reference voltage of 300 [V], and (3) reference voltage step change from 0 [V] to 300 [V]. The results shows that forward Euler-based MPC have a better dynamic response than improved Euler-based MPC.

5.1. Future work

Different alternatives are envisioned as future work. Some of them are the following:

- Extend the OSS-MPC strategy to control a 3L-NPC with output LCL filter.
- Study the performance of the control strategy with parallel connected 3L-NPC converters in standalone operation, such as an islanded microgrid.
- Design and implement state observers to predict the future value of the load current.
- Use better methods to choose the weighting factors of the cost function.

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Annexed A

RT Box and MCU Models

The MPC controller designed was tested using PLECS RT Box. The RT Box is an electronic device designed by PLEXIM to perform Hardware-in-the-Loop (HIL) simulation and Rapid Control Prototyping [87]. Its purpose is to allow engineers to test, implement and debug their control systems faster. This testing approach can help to reduce project cost and development time as errors are found and solved before deploying the control software with real power electronics hardware.

As mentioned, the RT Box has two modes of operation: HIL simulation and Rapid Control Prototyping. In HIL simulation, the RT Box emulates the behaviour of the power stage (i.e. the converter). Using his digital input pins, it receives the PWM signals from the microcontroller unit. These signals are used to compute the evolution of the continuous-time variables in real-time, and send it to the microcontroller through the analogue output pins. This process takes a few microseconds, thus tricking the MCU into thinking that it is controlling a real power electronics converter.

Rapid control prototyping is the opposite of HIL simulation. In rapid control prototyping, the RT Box is used to execute a control algorithm. In this mode of operation, the RT Box is connected to a power converter and send the appropriate PWM signals through the digital output pins. The sensors in the plant send the measurement signals through signal conditioning circuits to the analogue input pins of the RT Box. If the plant is not available, two RT Boxes can be connected back-to-back to simulate both systems.

In this appendix, the model of the plant and control algorithm will be explained. The converter was modelled using two methods. First, the model of the converter developed in Chapter 2 was used to describe its behavior. Then, components from PLECS library were used to model the converter. The model time step set for Real-Time simulation with the RT Box was 10 [μs].

A.1. The plant: RT Box Model

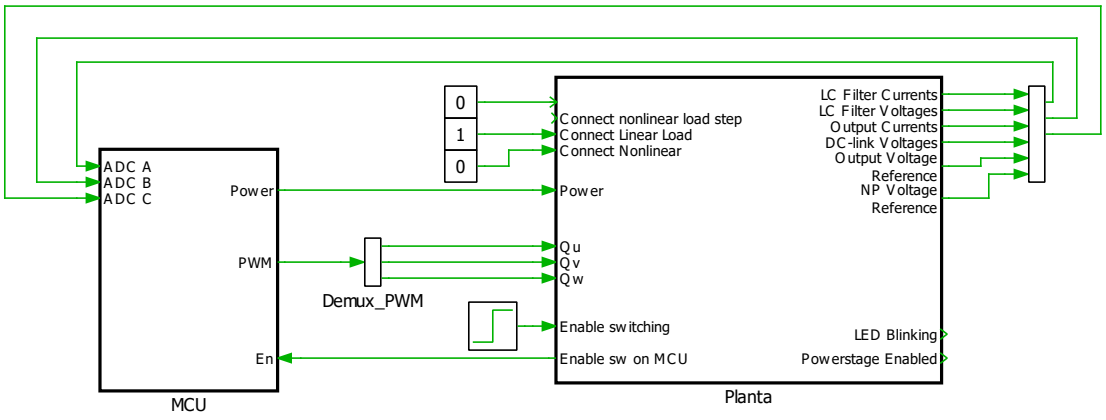

Figure A.1: Overview of the MCU and plant model built using PLECS Standalone.

In Fig. A.1, the subsystems for the power stage and microcontroller are shown. In this case, the RT Box is used for HIL simulation. The control algorithm is the device-under-test (DUT) and will be executed by the TMS320F28379D MCU from Texas Instrument. The plant and control algorithm model was separated into two subsystems to generate code separately for each. The generated code is then uploaded to the RT Box and MCU, respectively.

In Fig, A.2, the schematic of the plant is shown. In the schematic, we have the 3L-NPC with an LC filter connected to its AC output terminals. The 3L-NPC is built using 3 Three-Level Half-Bridge (NPC) modules from the Power Modules in PLECS Electrical library. The Three-Level Half-Bridge module (NPC) has two modes of operation: switched and sub-cycle averaged. During switched operation mode, all power semiconductors inside the module are modelled with ideal switches. The input signals to the module are the boolean digital signals generated by PWM modulation. On the other hand, the module in sub-cycle average operation is modelled with controlled voltage and current sources, see Fig. A.3. In sub-cycle average mode, the modules cannot model a shoot-through. Thus, the sum of the control signals for the first and third IGBT and second and fourth IGBT must not exceed 1 at any time.

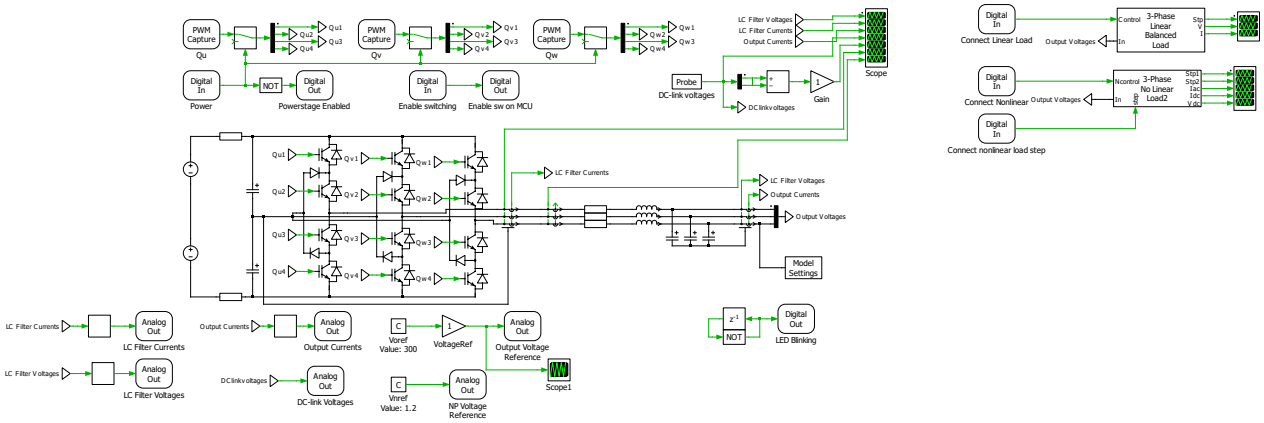

Figure A.2: Plant model in PLECS Standalone. The plant model is uploaded to the RT Box.

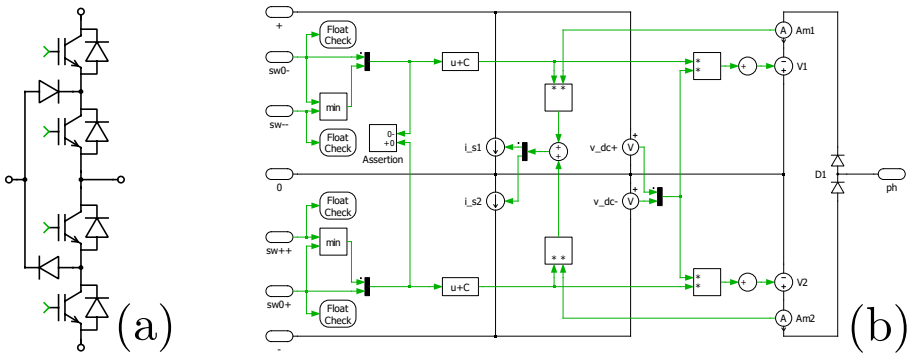

Figure A.3: Three-Level Half-Bridge (NPC) module and circuit of its sub-cycle average operation mode.

The PWM signals generated by the MCU are read using the PWM Capture Block. PLEXIM advises against the use of Digital Input Block to read PWM signals because they are slower than the PWM Capture block. The PWM Capture block averages the digital input over one model step. Its output is a signal in the range $[0, 1]$ corresponding to the percentage of time during which the digital input signal was active over the last model step period. The Three-Level Half-Bridge modules of the converter were set to sub-cycle average operation to deal with the continuous signal generated by the PWM capture blocks.

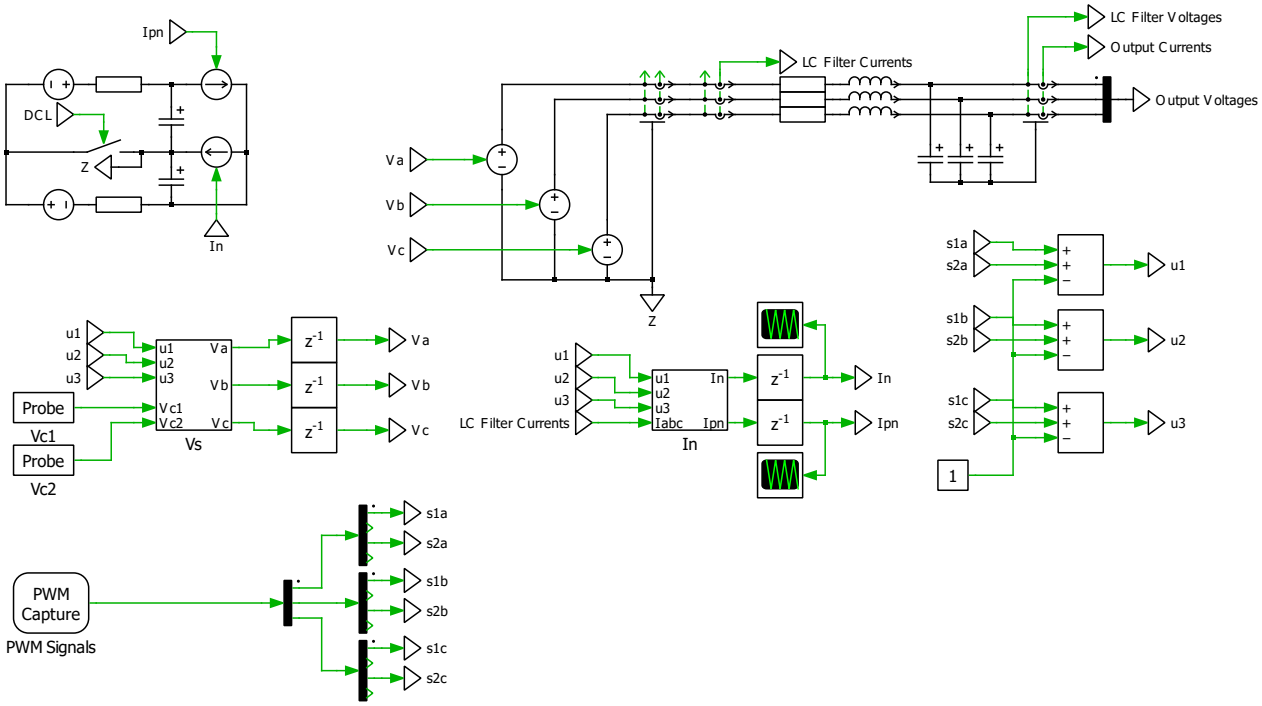

Figure A.4: 3L-NPC modelled with controlled voltage and current sources.

The 3L-NPC converter can also be described using the mathematical model developed in Chapter 2, as shown in Fig. A.4. The PWM Capture block receives the gating signals for all the power semiconductor devices of the converter. Using a Demux block, we separate the PWM signals of the main switching devices in each leg. Then, the leg switching state is computed as $u_x = u_{1x} + u_{2x} - 1$. In Fig. A.5(a), the model depicts eq. (2.1) to compute the output voltage. In Fig. A.5(b), the model computes the DC-link current and NP current.

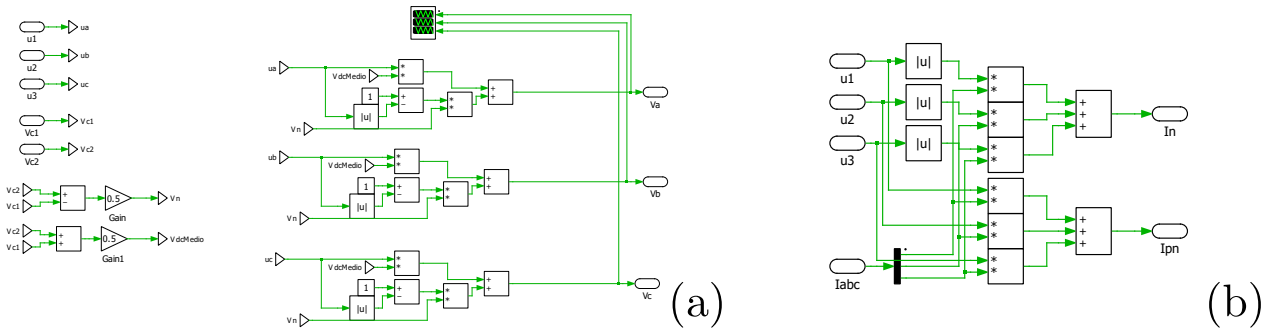

Figure A.5: Model used to compute the 3L-NPC output voltage, DC-link current, and NP current.

In Fig. A.6, the linear and nonlinear loads connected at the output of the LC filter are shown. The linear load is a three-phase resistor bank. The nonlinear load is a three-phase diode bridge rectifier. In the DC-side, a resistor is placed between the diode rectifier and the DC capacitor to limit the inrush current. The resistive load of the diode bridge is $R_n = 460$ [Ω]. To perform transient test of the nonlinear load, a resistance is placed in parallel to R_n through an ideal switch. The parallel resistance value is set to 32.093 [Ω]. Therefore, the equivalent resistance of the diode bridge is approximately 30 [Ω] when the switch is on.

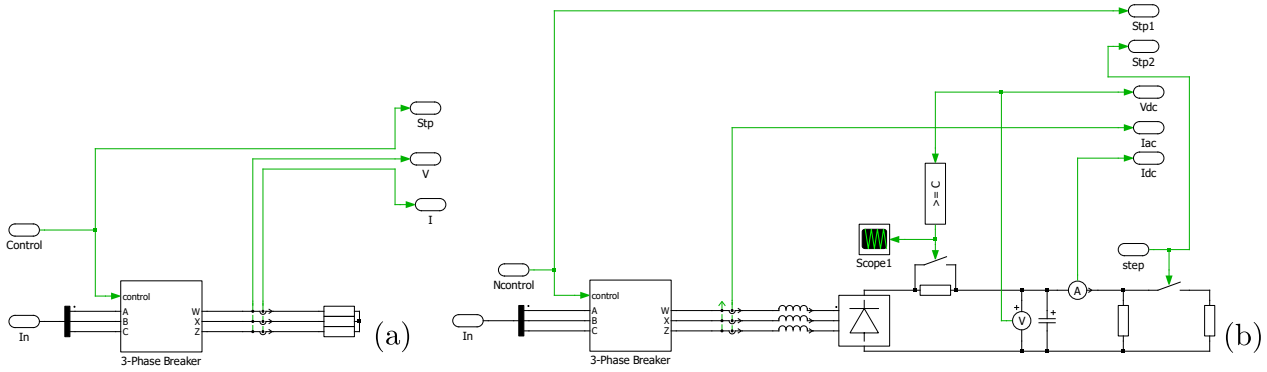

Figure A.6: Linear and nonlinear load connected to the output of the LC filter.

In Fig. A.7, the model of the three-phase breaker is shown. The breaker is used to connect and disconnect loads from the filter. The model consist of controlled voltage and current sources and a control signal. The line voltage at the input side is measured, transformed to phase voltage, multiplied by the control signal, and fed into the controllable voltage source at the output side. Then, the output current is measured and fed into the controllable current source at the input side. An alternative approach would be to connect the switches (one for each phase). However, that incremented the number of switching combinations in the model. Thus, increasing the computational complexity of the model.

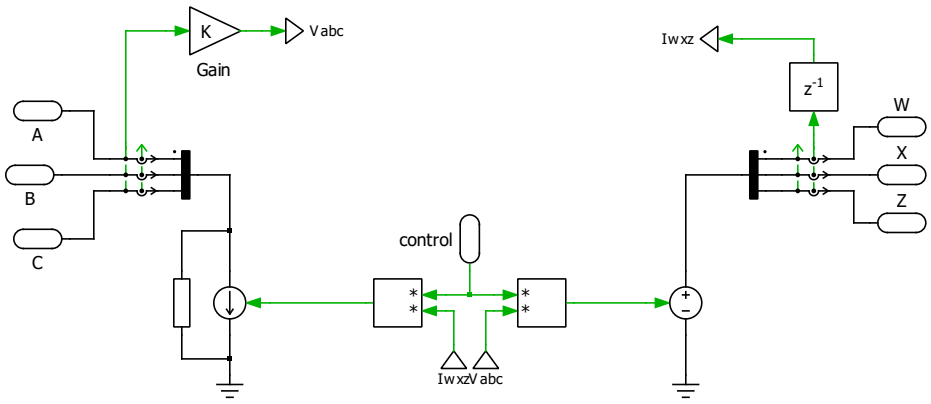

Figure A.7: Model of the phase breaker used to connected and disconnect loads from the system.

The measurements of the system variables are sent to the MCU through the analogue output channels. To sent signals through the analogue output channel, we have to use the Analog Output block. The block use a linear equation to map the measured signal to a range between $[0, 3.3]$ [V], see eq. (A.1). x and y are the input and output signals, respectively, and Q and O are the scale and offset factors. The scale and offset factors of various signals are shown in Table A.1.

$$y = \frac{3.0}{2Q}x + O \tag{A.1}$$

Table A.1: Scale and offset factors for different system variables sent through the analogue channel

Variable	Scale factor (Q)	Offset factor (O)
LC filter currents	15	1.5
LC filter voltages	400	1.5
Output currents	15	1.5
DC-link voltages	350	0
Output reference voltage	400	0
NP reference voltage	50	1.5

The LaunchXL-F28379D is placed over the LaunchPad Interface board designed by PLEXIM. The Launchpad Interface board have 4 sliding switchings, along with other features such as 8 BNC connetors to visualize analogue data in the oscilloscope. In this work, the four sliding switches were used in different tasks. Their signals are read from the RT Box using the Digital Input block. This approach is less computationally expensive than using digital switches in the model. In Fig. A.8, the task associated to each switch is shown.

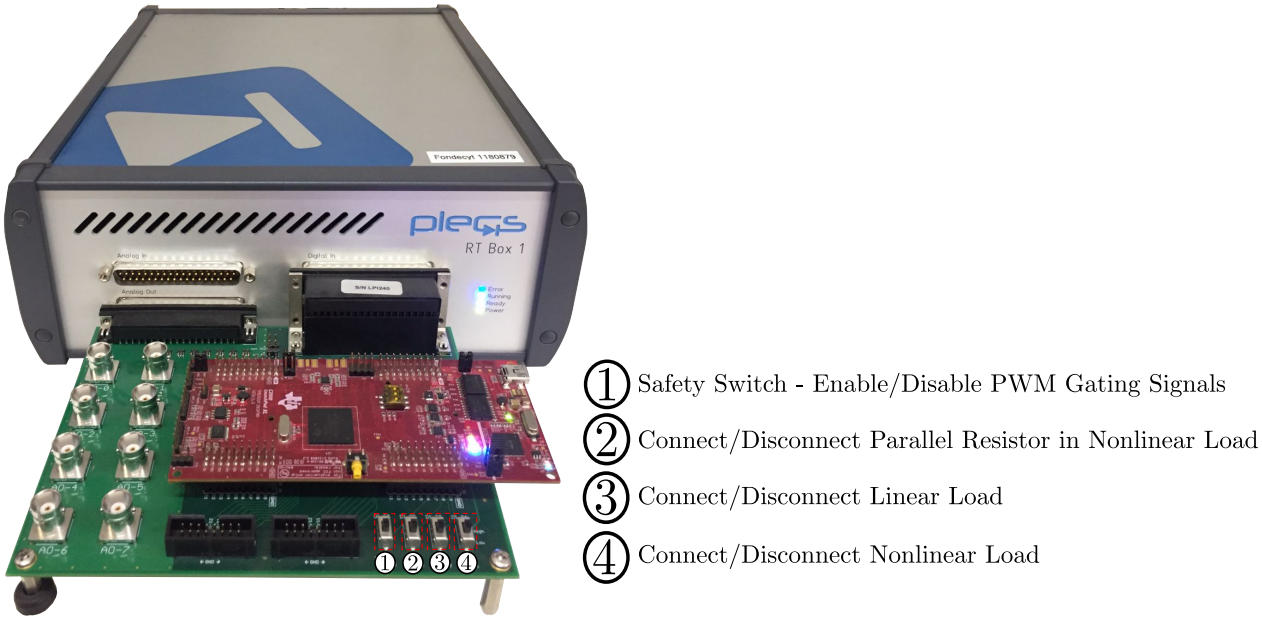

Figure A.8: Tasks assigned to the sliding switches in the LaunchPad Interface connected to the RT Box.

A.2. The controller: TMS320F28779D Model

In Fig. A.9, the model of the controller in the MCU is shown. The PWM block is connected to the ADC block to trigger the ADC Start of Conversion event. When the ADC finish conversion, the Control Task Trigger flag is set and the control algorithm begins to compute the gate signals for the next period.

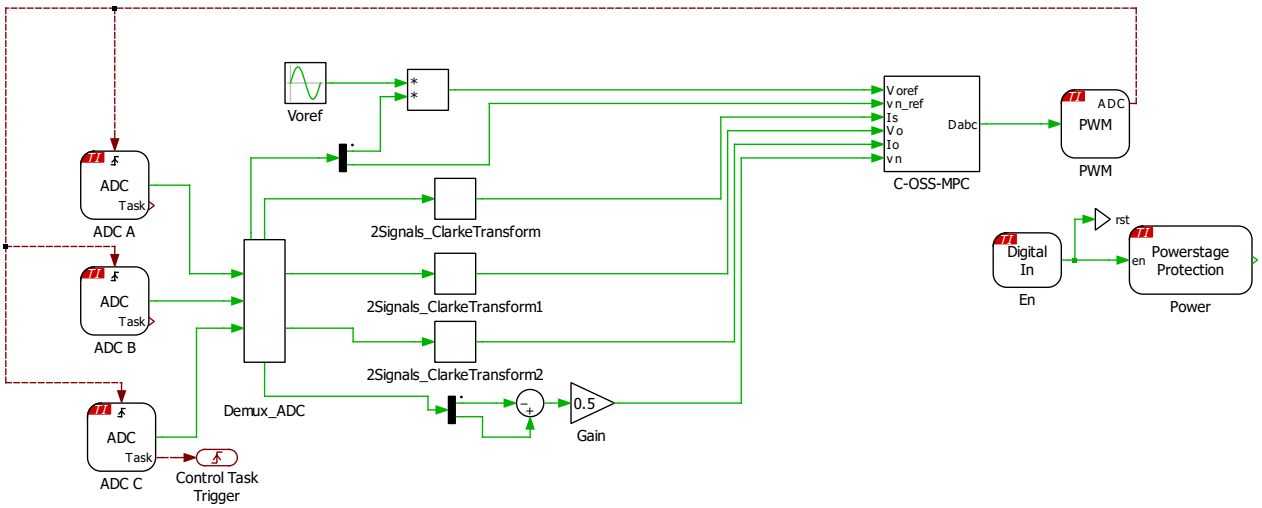

Figure A.9: Model of the controller in the MCU.

We reduced the number of analogue channels used taking measurements of only two of three phases in the AC side variables. Assuming that $x_a + x_b + x_c = 0$, we can simplify the Clarke transform. In eq. (A.2), the simplified Clarke transform is shown and in Fig. A.10 its implementation in the control algorithm is presented.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{\sqrt{3}}{3} & \frac{2\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \end{bmatrix} \tag{A.2}$$

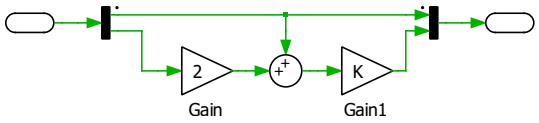

Figure A.10: Two-phase Clarke Transform built with PLECS blocks.

In Fig. A.11 the C-script used to implement the MPC algorithm is shown. The script takes as input the plant measurements, the limit for the amplitude of the converter reference current, and the weighting factors of the cost function. The output of the script is the three-phase modulation signal and the common-mode signal computed by the outer loop MPC to balance the neutral-point voltage. The three-phase modulation signal and the common-mode signal are added and passed to a transformation stage.

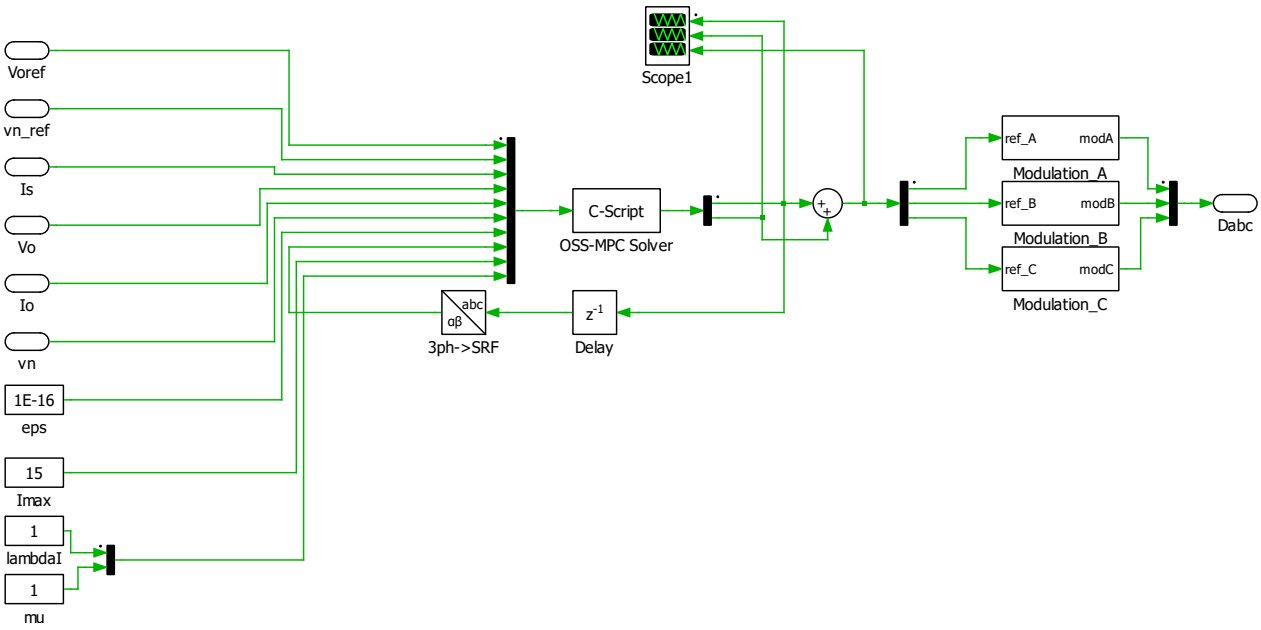

Figure A.11: Model of the MPC algorithm. The Algorithm is built using C language in the C-script.

The PWM module of the MCU compares the modulation signal with one triangular carrier to generate the gating signals of the converter. This CB-PWM is suitable for Two-Level inverters. However, the 3L-NPC uses two triangular carrier signals in phase but displaced along the vertical axis to generate the gatings signals for one leg. To achieve the 3L-NPC modulation scheme using single-carrier modulation, we break down the modulation signal from each phase into two signals.

Let m_x be the modulation signal computed by the controller for one converter leg, and m_{1x} and m_{2x} be the modulation signals for the independent semiconductor devices in the leg. The relationship between m_x and the modulation signals is described in eq. (A.3) and (A.4). An offset of 1 is added to m_{2x} to leave its range between $[0, 1]$. The implementation in PLECS is shown in Fig. A.12.

$$m_{1x} = \begin{cases} 1 & 0 < m_x \leq 1 \\ 0 & -1 \leq m_x \leq 0 \end{cases} \tag{A.3}$$

$$m_{2x} = \begin{cases} 0 & 0 < m_x \leq 1 \\ -1 & -1 \leq m_x \leq 0 \end{cases} \tag{A.4}$$

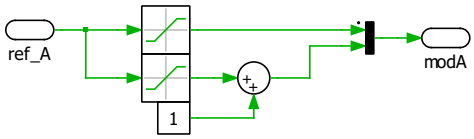

Figure A.12: Transformation of the three-phase modulation signal computed by the controller.

Annexed B

Simulation results of improved Euler-based controller with voltage weight factors

In this appendix, the performance of the system with improved Euler-based MPC and a voltage weight factor different than zero is studied. The voltage weight factor λ_v will be set to 0.02. Two case studies will be analized: considering $\lambda_u = 0$, and $\lambda_u = 4\mathbf{B}_d^\intercal \boldsymbol{Q} \mathbf{B}_d = 259.93$. The unconstrained control action $\boldsymbol{u}_{uc}$ for this case will be:

$$\boldsymbol{u}_{uc} = \begin{bmatrix} 0.011221 & 0 & 0.001496 & 0 \\ 0 & 0.011221 & 0 & 0.001496 \end{bmatrix} \boldsymbol{u}'_{db} + \begin{bmatrix} 0.8 & 0 \\ 0 & 0.8 \end{bmatrix} \boldsymbol{u}_{uss} \tag{B.1}$$

In Fig. B.1(a) and Fig. B.1(b), the load output voltage is shown for the system with forward Euler MPC and $\lambda_u = 0$. The load voltage cannot be controlled when forward Euler-based MPC and $\lambda_u = 0$ are used. This occurs because forward Euler discrete-time model does not have a direct relationship between the load voltage and the converter average switching vector. Consider the discrete-time input matrix $\mathbf{B}_d$ for forward Euler model:

$$\mathbf{B}_d = \begin{bmatrix} 7.291667 & 0 \\ 0 & 7.291667 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{B.2}$$

The last two rows in matrix $\mathbf{B}_d$ are used to map the average switching vector to the prediction of the load voltage one-step ahead. However, these last two rows have all its elements as zero when forward Euler model is used. This is not the case for improved Euler-based MPC. The latter can achieve output voltage control when $\lambda_u = 0$ because there exist a direct relationship between the load output voltage and the converter average switching vector in its discrete-time input matrix, as follows:

$$\mathbf{B}_d = \begin{bmatrix} 14.58318 & 0 \\ 0 & 14.58318 \\ 24.305556 & 0 \\ 0 & 24.305556 \end{bmatrix} \tag{B.3}$$

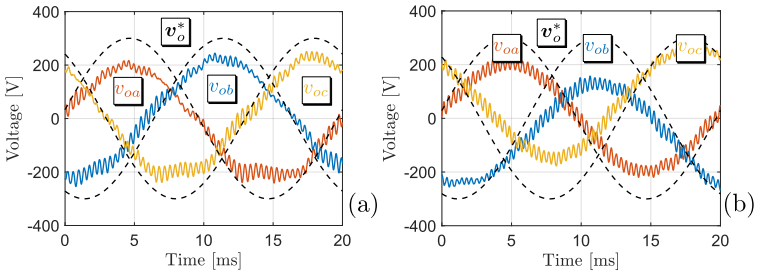

Figure B.1: Simulation result of the system with forward Euler model considering $\lambda_u = 0$. (a) Load output voltage without load at the output terminals, (b) Load voltage when a linear load is connected.

In Fig. B.2(a) and Fig. B.2(b), the load voltage for the system with improved Euler-based MPC and without load is shown. It can be seen that improved Euler with $\lambda_u = 0$ can achieve a good output voltage tracking, as shown by the instantaneous voltage error of Fig. B.2(b). The RMS voltage error for this case is 4.01 [V]. When λ_u increases, the instantenous voltage error decreases as can be seen in Fig. B.2(d). The RMS voltage is 3.01 [V] when $\lambda_u = 259.93$; thus, a reduction of 0.33 % in the average voltage error has been achieved. The controller has a better harmonic performance when $\lambda_u = 259.93$ is used, as seen in Table B.1. The THD and TDD of phase-to-neutral load voltage is 2.19 % and 2.18 %, respectively when the method with $\lambda_u = 0$ is used. When λ_u increases to 259.93, the THD and TDD for the phase-to-neutral load voltage have a value of 1.67 % and 1.66 %, respectively. Thus, a reduction of 0.52 % is achieved.

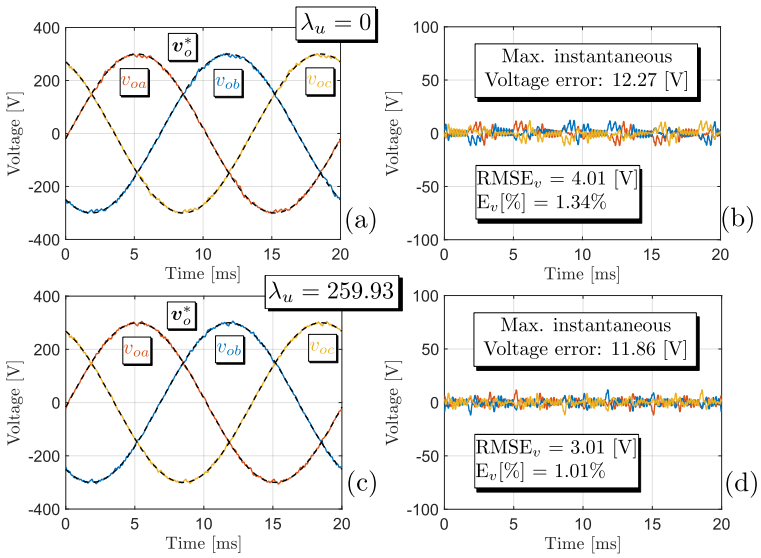

Figure B.2: Simulation result of the system with improved Euler model and no-load considering $\lambda_v = 0.02$. (a) Load output voltage, (b) Instantaneous voltage error.

In Fig. B.3(a) and B.3(b), the load voltage for the system with improved Euler-based MPC and a linear load is shown. It can be seen that improved Euler with $\lambda_u = 259.93$ has a better tracking and harmonic performance. The RMS voltage error for improved Euler with $\lambda_u = 0$ is 3.92 [V], as shown in Fig. B.3(b). Meanwhile, the RMS voltage error for improved Euler with $\lambda_u = 259.93$ is 2.56 [V], as shown in Fig. B.3(d). Thus, an improvement of 0.86 % in the average error is obtained. In Table B.1, the THD and TDD for the load voltage and current are shown. Improved Euler with $\lambda_u = 259.93$ achieves a reduction of 0.47 % in the load voltage THD and TDD, and a reduction of 0.47 % and 0.3 % in the load current THD and TDD.

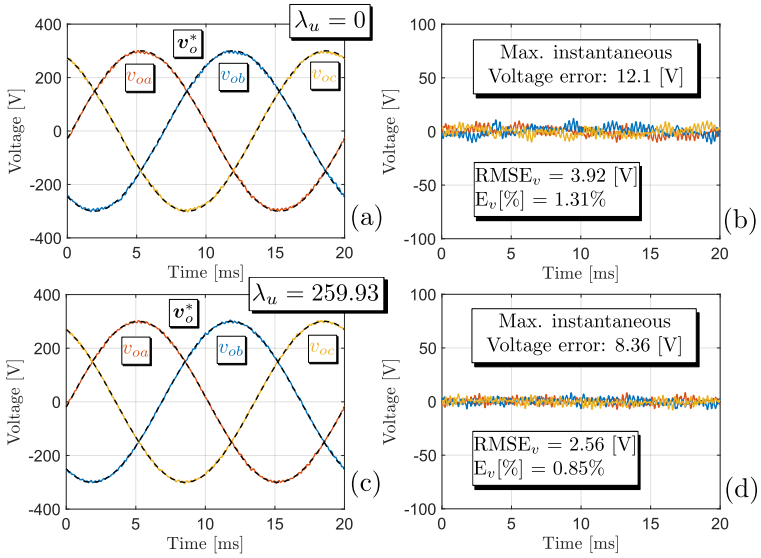

Figure B.3: Simulation result of the system with improved Euler model and linear load considering $\lambda_v = 0.02$. (a) Load output voltage, (b) Instantaneous voltage error, and (c) Load current.

In Fig. B.4(a) and B.4(b), the load voltage for the system with improved Euler-based MPC and a nonlinear load is shown. In this case improved Euler with $\lambda_u = 0$ has a better tracking and harmonic performance. The RMS voltage error for improved Euler with $\lambda_u = 0$ is 3.97 [V], as shown in Fig. B.4(b). Meanwhile, the RMS voltage error for improved Euler with $\lambda_u = 259.93$ is 5.2 [V], as shown in Fig. B.4(d). Thus, an increase of 0.4 % in the average error is obtained. In Table B.1, the THD and TDD for the load voltage and current are shown. Improved Euler with $\lambda_u = 259.93$ increases in 0.6 % the load voltage THD and TDD, and a reduction of 0.75 % in the load current THD.

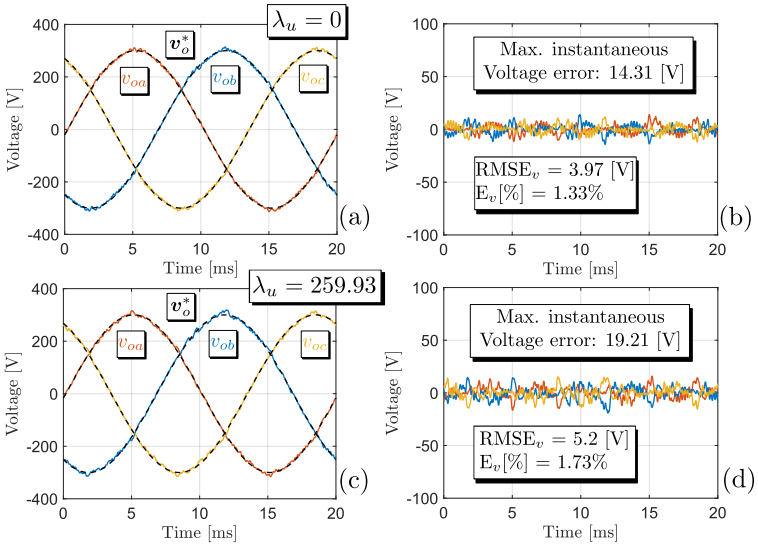

Figure B.4: Simulation result of the system with improved Euler model and nonlinear load considering $\lambda_v = 0.02$. (a) Load output voltage, (b) Instantaneous voltage error, and (c) Load current.

Table B.1: THD and TDD for load voltage and current for improved Euler-based MPC with different weights.

Improved Euler-based MPC with $\lambda_v = 0.02$ and $\lambda_u = 0$						
Condition	THD phase-to-neutral Load voltage	TDD phase-to-neutral Load voltage	THD line-to-line Load voltage	TDD line-to-line Load voltage	THD load current	TDD load current
No load	2.19	2.18	2.19	2.18	-	-
Linear load	1.89	1.87	1.89	1.87	1.89	1.24
Nonlinear load	2.31	2.31	2.31	2.31	95.67	7.54
Improved Euler-based MPC with $\lambda_v = 0.02$ and $\lambda_u = 259.93$						
No load	1.67	1.66	1.67	1.66	-	-
Linear load	1.42	1.41	1.42	1.41	1.42	0.94
Nonlinear load	2.79	2.79	2.79	2.79	94.92	7.53

Finally, the transient response of the system will be studied. In Fig. B.5(a) and Fig. B.5(b), the system is working at 300 [V] without load when a linear load is connected. In Fig. B.5(a), improved Euler MPC with $\lambda_u = 0$ is used to control the converter. Meanwhile, in Fig. B.5(b) the value of λ_u was increased to 259.93. It can be seen that improved Euler with $\lambda_u = 0$ has a slower dynamic response. It takes 0.74 [ms] for the system to arrive at the voltage band around the reference value. Meanwhile, increasing λ_u produce a faster dynamic response in this case. The settling time in Fig. B.5(b) is 0.51 [ms]. Thus, increasing the weight factor associated to the control effort allows a faster recovery for the system when a linear load is connected. However, it also increases slightly the voltage dip. Then, in Fig. B.5(c) and

B.5(d), the transient response for a voltage reference step change is shown. It can be seen that improved Euler with $\lambda_u = 0$ present a faster dynamic response in this case, contrary to the case when a linear load is connected. Also, increasing the value of λ_u produce an oscillatory response characteristic of second-order systems.

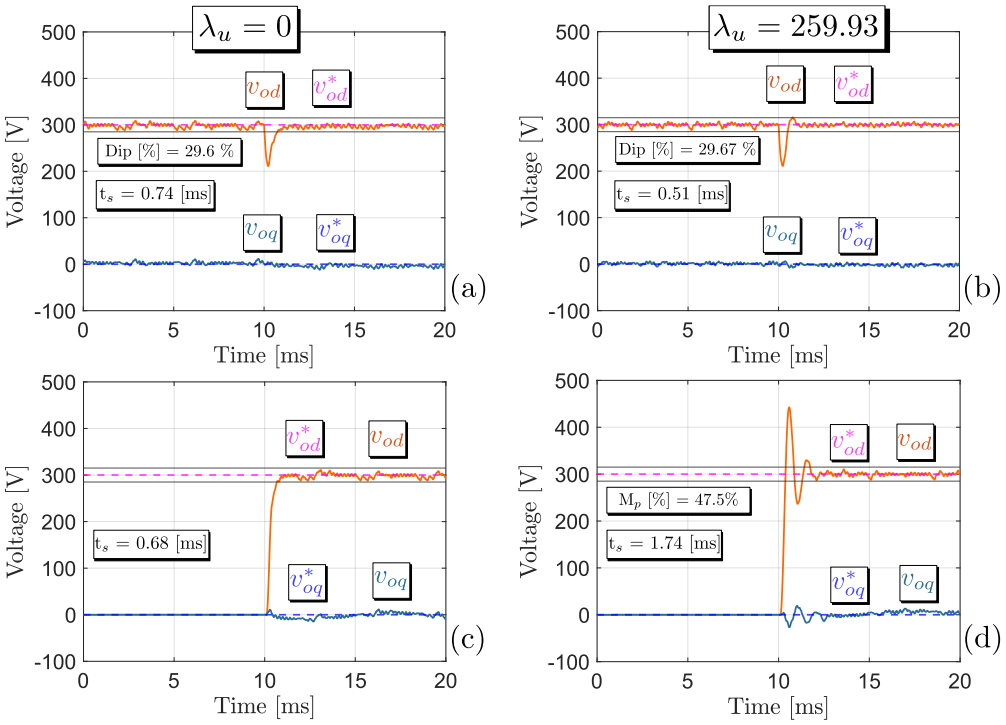

Figure B.5: Simulation result of the controller with improved Euler model during transient response considering $\lambda_v = 0.02$. (a) Load step transient with $\lambda_u = 0$, (b) Load step transient with $\lambda_u = 259.93$, (c) Voltage step transient with $\lambda_u = 0$, (d) Voltage step transient with $\lambda_u = 259.93$.