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Unipolar resistive switching behavior in Al_2O_3/HfO_2 multilayer dielectric stacks: fabrication, characterization and simulation

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Abstract

In this work, the impact of different HfO_2/Al_2O_3-based multilayer dielectric stack (DS) configurations on the electrical characteristics and on the resistive switching (RS) performance of Ni/Insulator/Silicon devices has been systematically investigated. Significant differences are observed in the electrical characteristics of the fabricated bilayer, trilayer and pentalayer stacks compared to a single HfO_2 layer of the same physical thickness. The RS analysis has shown similar low resistance state currents and set voltages for all the DS combinations whereas currents at the high resistance state and reset voltages depend on the DS. The shift of the reset voltage to lower values for HfO_2 and $Al_2O_3/HfO_2/Al_2O_3$ cases is explained by the results from thermal simulations that reveal that these differences could be associated to the different temperature distributions at the narrowest part of the conductive filament immediately before the thermally triggered reset process occurs.

Supplementary material for this article is available online

Keywords: ALD, HfO_2, Al_2O_3, resistive switching, multilayer dielectric stacks, thermal simulations, nanolaminates

(Some figures may appear in colour only in the online journal)

1. Introduction

Devices based on the resistive switching (RS) phenomenon are currently being investigated for applications such as non-volatile resistive random access memories [1], synapses in neuromorphic computing [2, 3] or physical unclonable functions for security applications [4, 5]. Among the possible alternatives, RS devices based on HfO_2 have shown fast switching times, high endurance, low energy consumptions, CMOS compatibility, and an excellent capability to modulate their electrical resistance [3, 6]. In addition, several works [7–14] have shown the advantage of using HfO_2/Al_2O_3 stack combinations in RS devices to enhance their electrical properties. For instance, Azzaz *et al* [7], have published the improvement of the device endurance and data retention when a thin layer of Al_2O_3 is added to a single HfO_2 layer. Yu *et al* [8], have demonstrated an improved multilevel capability of HfO_x/AlO_x bilayer stacks under DC and AC conditions. Furthermore, $Al_2O_3/HfO_2/Al_2O_3$ trilayer stacks have been reported to have excellent RS performances with low parameter dispersion [9] and an improved multilevel cell operation by controlling reset stop voltages and good switching characteristics under AC condition [10]. Besides that, other groups have demonstrated RS behavior and performance

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improvements in HfO_2/Al_2O_3 multilayers employing more than three layers. Among them, Tzeng *et al* [11] have reported both positive and negative unipolar RS behavior of HfO_2/Al_2O_3-based multilayers observing differences in switching and stability characteristics between the two operation modes. In addition, Huang *et al* [12] implemented HfO_2/Al_2O_3 multilayer stacks in RRAM arrays showing an improved tail-bit retention compared to single layer HfO_2RRAM.

This work is focused on unipolar RS devices with Ni as metal electrode where the high temperature on the reset process due to joule heating is the most predominant cause for the rupture of the conductive filament (CF) [15]. Notice that Ni migration in the dielectric, facilitates the formation of metallic filaments, which is thermally and voltage induced [16]. In [13], Tran *et al* reported in unipolar Ni-based RRAM devices a reduced switching variability and an increased resistance ratio between two states when using a HfO_x/AlO_y bilayer stack compared to a single HfO_x layer. The order of a HfO_2/Al_2O_3 bilayer, however, was reported to have no impact on Ni-based RRAM characteristics [14].

Although some studies have dealt with the RS behavior in HfO_2/Al_2O_3 multilayer dielectric stacks (DS), no performance comparisons in an extended set of several multilayer stack configurations have been reported, being difficult to isolate the contribution of the DS on the device performance from the contribution of the other processing steps in the fabrication process. Thus, in this work, unipolar RS devices with Ni top electrode and bilayer, trilayer and multilayer (pentalayer) DS combining and alternating HfO_2/Al_2O_3 layers have been fabricated and systematically characterized to study in depth the impact of different dielectric configurations on the electrical characteristics and on the RS performance. In addition, the experimental results are combined with physical simulation to further understand the role of the DS on the device performance. To this end, the capacitance–voltage and current–voltage characteristics have been first measured and analyzed. Then, a RS assessment of all DS has been carried out, including the analysis of the cycle-to-cycle variability. Finally, combining the experimental RS results and analysis together with thermal simulations of the devices, the thermal response of the fabricated structures has been studied. In this respect, a comprehensive investigation on the thermal behavior is done making use of a simulation tool that solves the 3D heat equation in a detailed manner.

2. Device fabrication

The fabricated metal–insulator–semiconductor (MIS) devices are field-oxide isolated Ni/insulator/Si-n$^+$ square structures with active areas ranging from 480 × 480 to 5 × 5 μm^2. A cross sectional view is shown in figure 1. The devices were fabricated on highly doped n-type (100) Czochralski silicon wafers with a resistivity in the range (0.007–0.013) Ω cm. After a standard wafer cleaning, a 200 nm thick SiO_2 layer was grown by means of a wet thermal oxidation process at 1100 °C. This field oxide was patterned by photolithography and wet etching. Prior to insulator deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in HF(5%) were done. The oxide layers were grown at 225 °C by atomic layer deposition (ALD) in a Cambridge NanoTech Savannah 200 system. The precursors used were trimethylaluminium, (TMA) and H_2O for Al_2O_3, and tetrakis(dimethylamido)-hafnium (TDMAH) and H_2O for HfO_2. N_2 was employed as carrier and purge gas. Al_2O_3 and HfO_2 layers were combined to build bilayer, trilayer and pentalayer DS all of them with a total physical thickness of 20 nm. Samples with a 20 nm thick HfO_2 layer were also fabricated for comparison purposes. Figure 2 shows the studied DS combinations referred to as DS1 to DS6. The top metal electrode of the fabricated devices consists of a 200 nm thick Ni layer deposited by magnetron sputtering and patterned by a lift-off process.

The ALD technique provides excellent thickness control and uniformity. The oxide thickness can be obtained by adjusting the number of ALD cycles [17] to grow a HfO_2 layer of 20, 10, 5 or 4 nm, the ALD consisted in 210, 105, 55 and 36 ALD cycles. Analogously, 91, 45 and 36 ALD cycles were used to grow Al_2O_3 layers of 10, 5 and 4 nm, respectively. An example of the ALD reactor pressure in the deposition process carried out to obtain the trilayer DS (5 nm-Al_2O_3/10 nm-HfO_2/5 nm-Al_2O_3) is shown in figure 3.

TEM inspections of 20 nm thick HfO_2 layers indicate that they are polycrystalline [18], while ALD grown Al_2O_3 films are amorphous.

3. Impact of the multilayer stack on the electrical characteristics and dielectric reliability

A first electrical characterization of the fabricated MIS devices was performed through the measurement and analysis of the high-frequency capacitance–voltage (C–V) characteristics. In order to obtain reliable capacitance measurements, devices with an area of 480 × 480 μm^2 were used. The C–V measurements were carried out at 100 kHz signal frequency by sweeping the voltage from inversion to accumulation using an HP4192A impedance analyzer in parallel configuration. Figure 4 shows representative C–V characteristics of the studied DS. From the experimental C–V curves, the equivalent oxide thickness (EOT), defined as the required thickness of a silicon dioxide film to achieve the same capacitance density as the high-k material [19], was extracted for the different DS from the following equation:

$$C_{\text{max,high-}k} = \frac{\varepsilon_0 k_{SiO_2}}{\text{EOT}} A, \quad (1)$$

where C_{max} is the maximum capacitance measured at the accumulation region, ε_0 the vacuum permittivity, k_{SiO2} the relative dielectric constant of SiO_2, and A the capacitor area. From equation (1), for a high-k layer of physical thickness $t_{\text{high-}k}$, EOT is related to it by the following relationship:

$$\text{EOT} = \frac{k_{SiO_2}}{k_{\text{high}-k}} t_{\text{high-}k}. \quad (2)$$

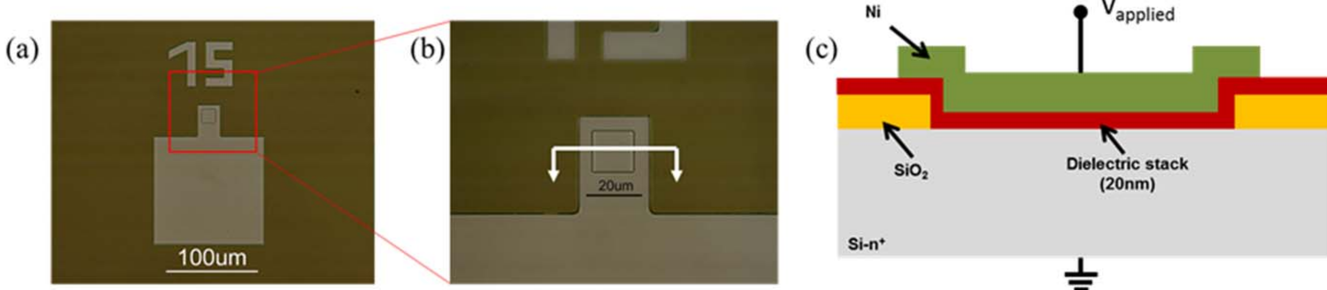


Figure 1. Optical image of (a) the top view of a fabricated MIS device and (b) zoom of the active area. (c) Schematic cross section of the device along the white line indicated in (b).

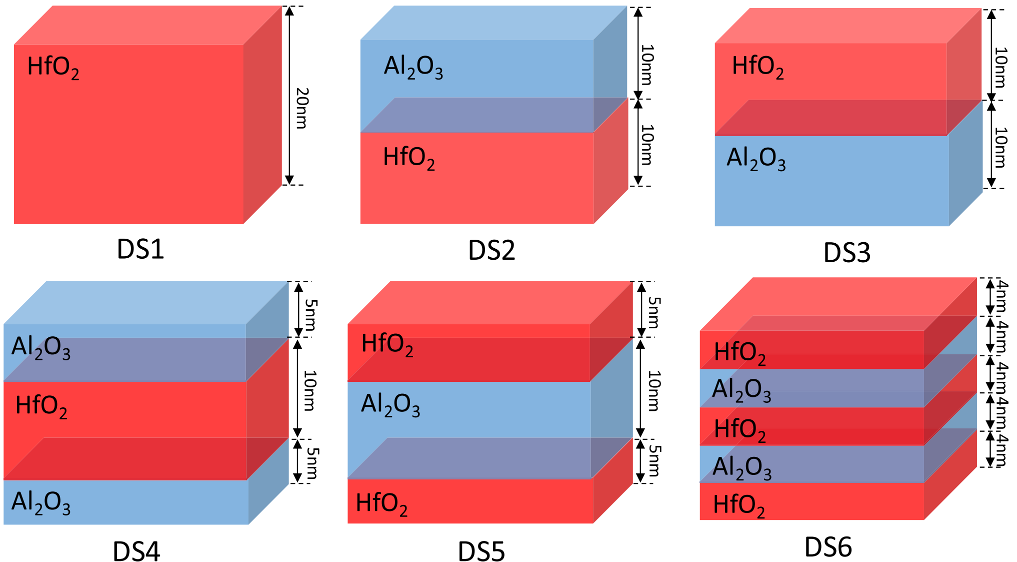


Figure 2. Fabricated HfO_2 and HfO_2/Al_2O_3-based dielectric stacks (DS) combinations labeled from DS1 to DS6.

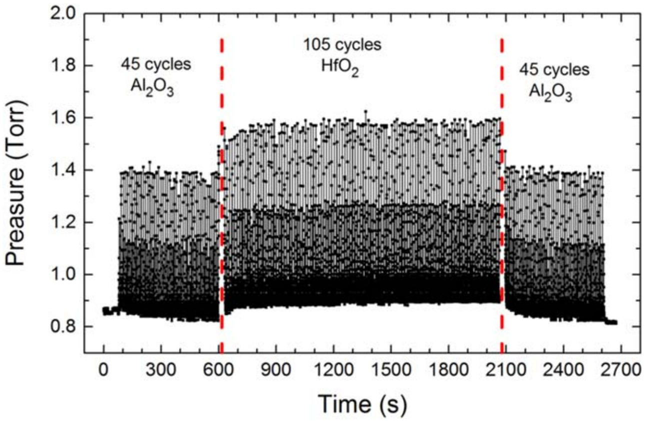


Figure 3. Reactor pressure of the atomic layer deposition (ALD) process for the 5 nm-Al_2O_3/10 nm-HfO_2/5 nm-Al_2O_3 trilayer stack.

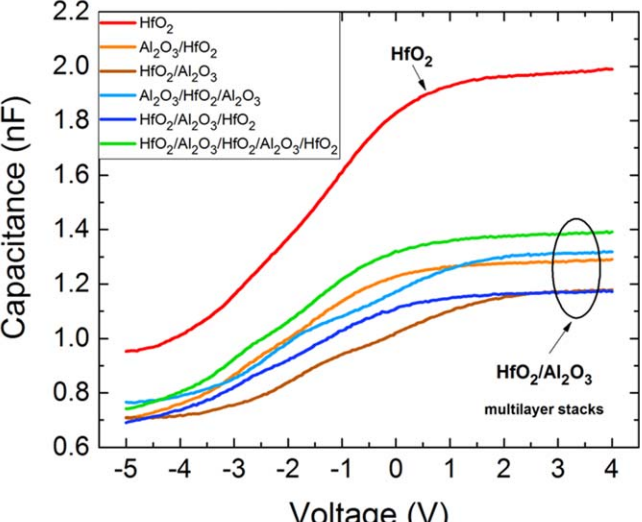


Figure 4. *C–V* characteristics at 100 kHz for the different dielectric stack combinations. Device area is $480 \times 480\ \mu m^2$.

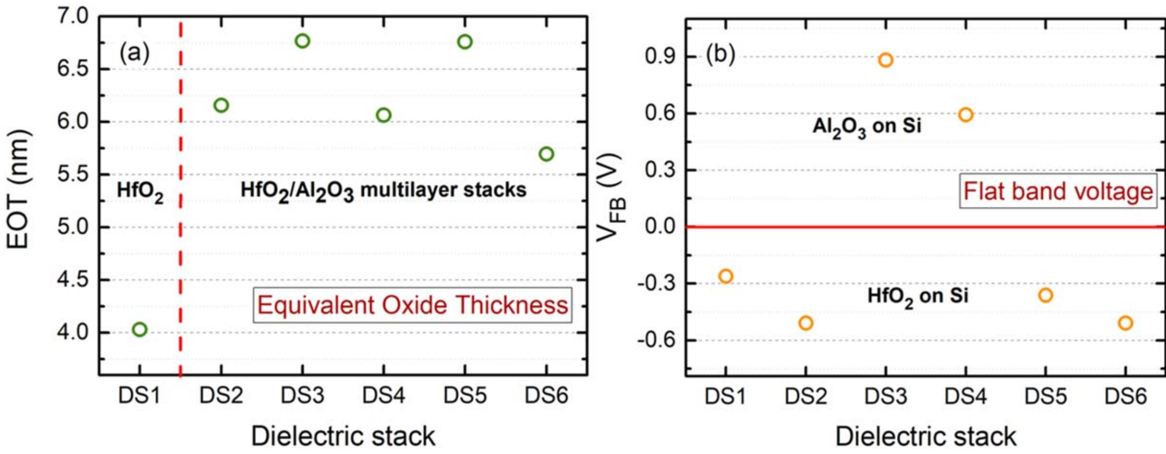


Figure 5. Extracted (a) equivalent oxide thickness (EOT) and (b) flat band voltage (V_{FB}) parameters from the high-frequency *C–V* characteristics.

In figure 5(a), where the obtained values for EOT are depicted for the different stacks, it is shown that the inclusion of Al_2O_3 in a multilayer stack leads to larger EOT values compared to a single HfO_2 layer. Considering equation (2), this result is in accordance with the lower dielectric constant of Al_2O_3 (∼9) compared to HfO_2 (∼25). Notice that all the stacks have a physical thickness of 20 nm. In addition, in the case of multilayer stacks, similar EOT values were obtained for the different combinations; the smallest one corresponds to the pentalayer stack (DS6 split). This result is due to the fact that, in this case, the thickness ratio $t_{HfO_2}/t_{Al_2O_3}$ is 3/2, while in the other cases the ratio is 1.

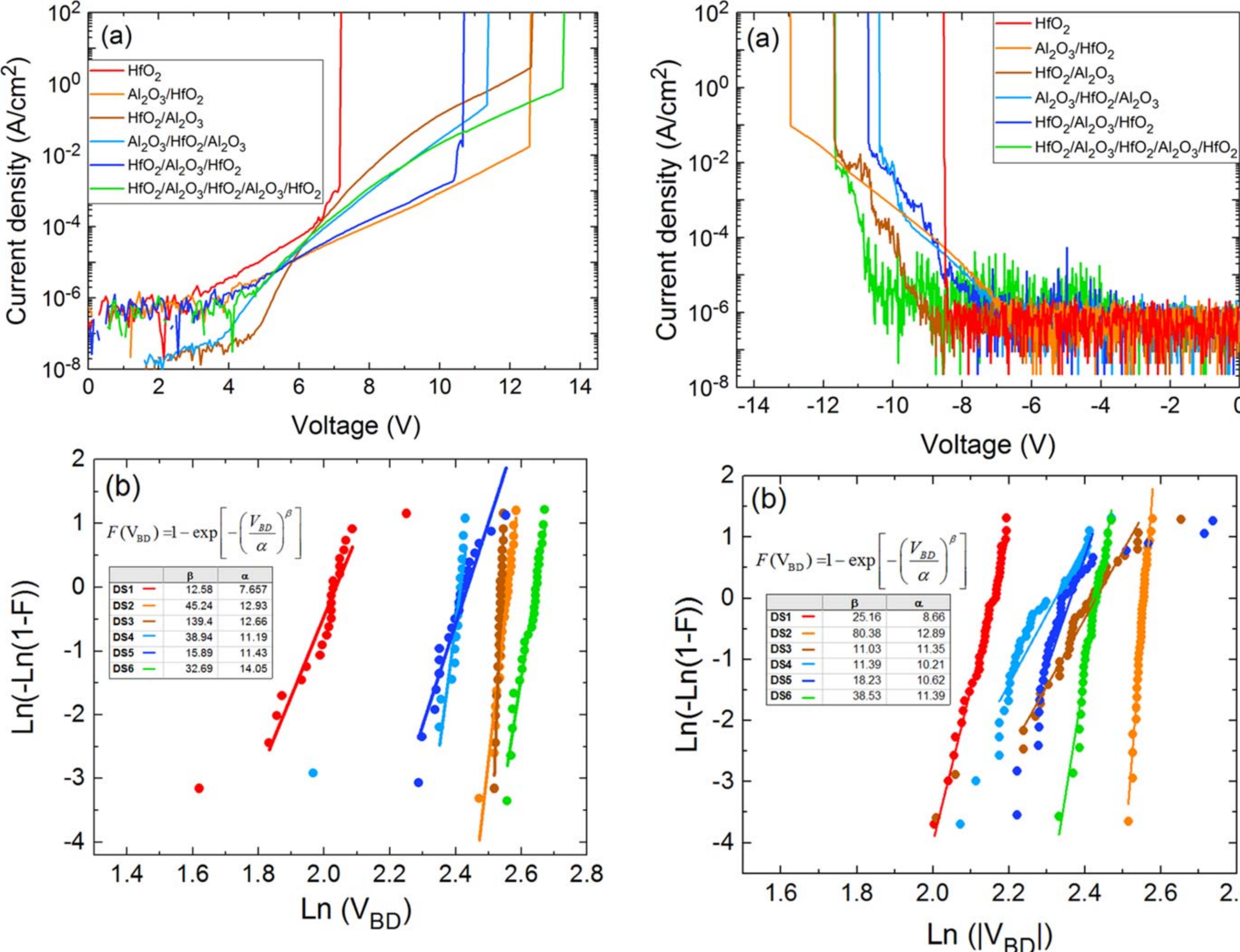
In addition, from the experimental *C–V* curves, the flat band voltage (V_{FB}) was determined from the flat band capacitance (C_{FB}) and considering the series connection of the oxide capacitance (C_{ox}) and the flat band semiconductor capacitance. C_{FB} [20] is then given by:

$$C_{FB} = \frac{A}{\frac{A}{C_{ox}} + \frac{L_D}{\varepsilon_s}}, \quad (3)$$

where L_D is the Debye length, ε_s is the silicon dielectric constant and A the device area. The extracted V_{FB} values, shown in figure 5(b), indicate that for those DS with an Al_2O_3 layer adjacent to the silicon substrate (DS3: HfO_2/Al_2O_3 and D6: $Al_2O_3/HfO_2/Al_2O_3$) V_{FB} is positive whereas for those with a HfO_2 layer deposited on the silicon substrate V_{FB} is negative. This result is consistent with the larger fixed negative charge reported in Al_2O_3 layers compared to HfO_2 [21]. This fixed negative charge in Al_2O_3 films can be attributed to Al vacancies, O interstitials, and interstitial H, because of the H containing ALD precursors TMA ($Al(CH_3)_3$) and H_2O [22]. In addition, the presence of fixed negative charge in Al_2O_3 layer has also been reported to be influenced by *C*-related impurities [23].

With respect to assessing the electrical conduction through the different DS, current–voltage (*I–V*) measurements were performed using an HP4155 semiconductor parameter analyzer on pristine devices with an area of 15 × 15 μm^2. The voltage was applied to the Ni top electrode, while the Si substrate was grounded. Voltage sweeps were applied from 0 V up to the occurrence of the dielectric breakdown for both polarities. Since these type of devices need to be subjected to a forming process before the RS phenomenon is observed, the obtained *I–V* characteristics are representative of the forming behavior of the studied devices in both polarities. Figures 6(a) and 7(a) show typical *I–V* curves for each DS under substrate (positive bias) and gate (negative bias) injection regimes, respectively. Under substrate injection (figure 6(a)), devices with a single HfO_2 layer exhibit larger currents than multilayer stacks at voltages values below ∼7 V (figure 6(a)). This fact could be related to the lower conduction band offset (barrier height) between the silicon substrate and the insulator layer in the case of HfO_2 (∼1.4 eV) case than in Al_2O_3 (∼2.5 eV) [24]. For larger voltages (>7 V), the HfO_2/Al_2O_3 stack presents the largest current while Al_2O_3/HfO_2 and $HfO_2/Al_2O_3/HfO_2$ stacks show the smallest. This difference is in accordance with the work carried out in [14], where the dielectric conduction in Al_2O_3/HfO_2 and HfO_2/Al_2O_3 bilayer stacks was compared. Under gate injection (figure 7(a)), no dielectric conduction is observed in any stack for voltage values below |−7 V|. However, at larger voltages, higher current values are observed for the trilayer cases in comparison to the other multilayer stacks.

Comparing the current behavior at large voltages (∼|8 V|) independently of the injection regime, stacks with Al_2O_3 adjacent to the injecting electrode show larger current than those having HfO_2. The explanation of such a result is given by the analysis of the band diagram carried out for every multilayered stack. In the case of the Al_2O_3 layer located next to the injecting electrode and the device positively or negatively biased, electrons only find an Al_2O_3 barrier with triangular shape and once overcome no further barrier is found and, therefore, larger conduction is possible. However, when HfO_2 is the adjacent layer, electrons encounter two barriers the first due to the HfO_2 layer and the second to the contiguous Al_2O_3 layer, since Al_2O_3 has a larger bandgap (8.7 eV) than HfO_2 (5.7 eV). Notice that this double HfO_2/Al_2O_3 barrier can be double triangular shaped or even a combination of a trapezoidal and a triangular shape



	β	α
DS1	12.58	7.657
DS2	45.24	12.93
DS3	139.4	12.66
DS4	38.94	11.19
DS5	15.89	11.43
DS6	32.69	14.05

	β	α
DS1	25.16	8.66
DS2	80.38	12.89
DS3	11.03	11.35
DS4	11.39	10.21
DS5	18.23	10.62
DS6	38.53	11.39

Figure 6. (a) Current–voltage characteristics for positive bias (substrate injection) up to dielectric breakdown. (b) Weibull plot of the cumulative breakdown distribution function F versus breakdown voltage, V_{BD} in V. The extracted shape (β) and scale (α) parameters of the Weibull function for the different dielectric stacks are shown in the inset table. Device area is $15 \times 15\ \mu m^2$.

Figure 7. (a) Current–voltage characteristics for negative bias (top electrode injection) up to dielectric breakdown. (b) Weibull plot of the cumulative breakdown distribution function F versus |breakdown voltage| (V_{BD} in V). The extracted shape (β) and scale (α) parameters of the Weibull function for the different dielectric stacks are shown in the inset table. Device area is $15 \times 15\ \mu m^2$.

what makes the conduction more difficult and leads to a lower current.

In order to evaluate the reliability of HfO_2/Al_2O_3 multilayer stacks compared to a single HfO_2 layer, the dielectric breakdown has been studied. For this purpose, ramped *I–V* characteristics of a set of more than 25 capacitors of each type and for each polarity were measured and the breakdown voltage (V_{BD}) was recorded. Comparison of the obtained results is carried out through the analysis of the Weibull cumulative breakdown distributions (figures 6(b) and 7(b)) defined as:

$$F(V_{BD}) = 1 - \exp\left[-\left(\frac{|V_{BD}|}{\alpha}\right)^{\beta}\right], \tag{4}$$

where α is the voltage at which 63.2% of the capacitors are broken, and β is the Weibull slope, which indicates the width of the distribution. The obtained α and β values are shown in the inset table of figure 6(b) (positive polarity) and figure 7(b) (negative polarity). It can be noticed that for both polarities the lowest breakdown voltage corresponds to the single HfO_2 layer compared to multi-layered dielectrics (figures 6(a) and 7(a)), resulting in a significantly smaller α parameter. In addition, among the Al_2O_3/HfO_2 stack combinations, both trilayer stacks show the lowest α parameter under both polarities, while the β parameter shows no clear trend.

The analysis of the electrical characteristics and dielectric reliability in pristine devices have demonstrated the different physical properties of the fabricated multilayered stacks. These results confirm that prior to the forming process, the insulator films show dissimilar capacitance and conduction behavior.

4. Effect of the DS on the RS phenomenon

Having observed significant differences in the electrical characteristics of the different stacks, RS behavior is next studied in order to analyze the impact of the type of stack on

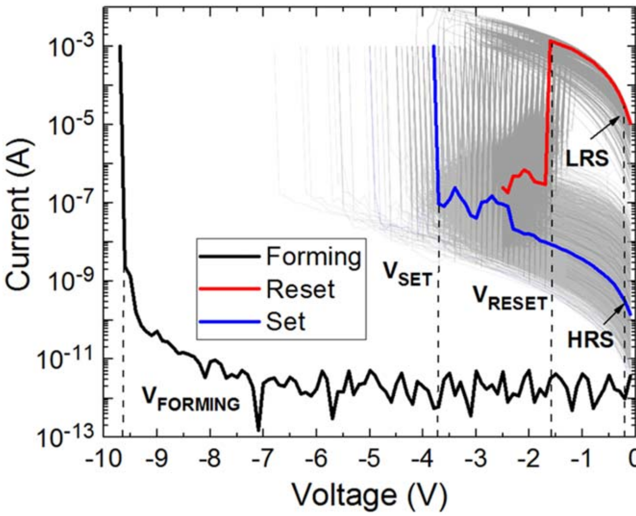


Figure 8. Experimental *I–V* curves for the forming process and 2000 cycles of negative unipolar RS for the $Al_2O_3/HfO_2/Al_2O_3$ stack. HRS, LRS, $V_{FORMING}$, V_{SET} and V_{RESET} parameters are indicated. Device area is $5 \times 5\ \mu m^2$.

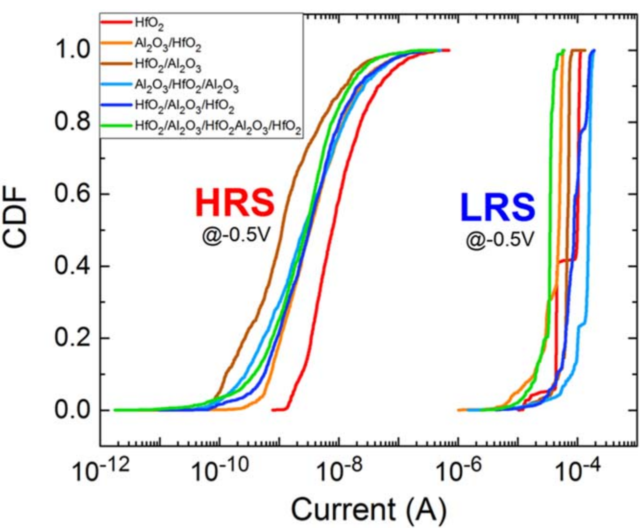


Figure 9. Experimental cumulative distribution functions of the HRS and LRS currents, extracted at −0.5 V, corresponding to a set of 2000 RS cycles.

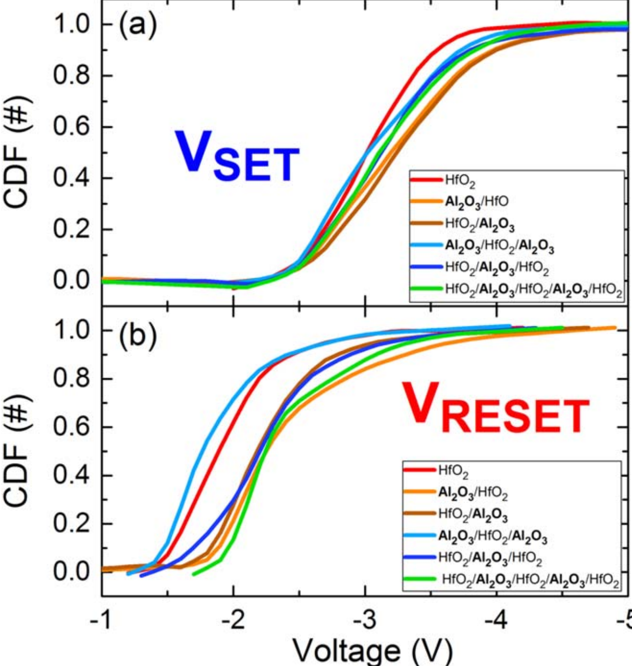


Figure 10. Experimental (a) set and (b) reset voltage cumulative distribution functions obtained from 2000 RS cycles for each of the different dielectric stacks.

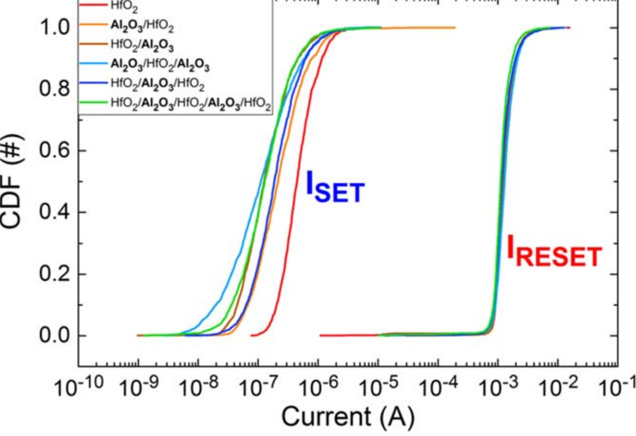


Figure 11. Experimental cumulative distribution functions of the set and reset currents obtained from 2000 RS cycles for each of the different dielectric stacks.

the RS performance. Previous works on Ni-based devices with a single HfO_2 layer [25–27] reported better RS performance under negative unipolar conditions in comparison to other polarity combinations. Under such conditions, by applying negative voltage ramps, a metallic-like CF is formed (set process) and disrupted (reset process) [28]. According to [15, 27], the formation of the CF is due to metallic diffusion through the oxide layer from the top electrode into the dielectric, while the disruption of CF is known to be a temperature-driven rupture of the filament [2, 29–31].

4.1. RS assessment

In order to study the negative unipolar RS performance of the devices, as the first and necessary step, they were subjected to a forming process under negative polarity with a current limitation of 1 mA in order to form the CF but preventing the hard and irreversible dielectric breakdown. In our previous work [32], it was shown that the CF is most likely to be created within the active area of the device rather than at the edge. With the purpose of reducing the variability of the switching process, devices with an area of $5 \times 5\ \mu m^2$ were used. Then, 2000 consecutive reset-set cycles were performed applying negative voltage sweeps to drive the device to the high resistance state (HRS) and to the low resistance state (LRS), alternatively. It should be noted that in the set processes a current limitation of 1 mA was imposed to prevent hard breakdown whereas the reset process was performed without current limitation. RS measurements were carried out using a B1500 semiconductor parameter analyzer. As an

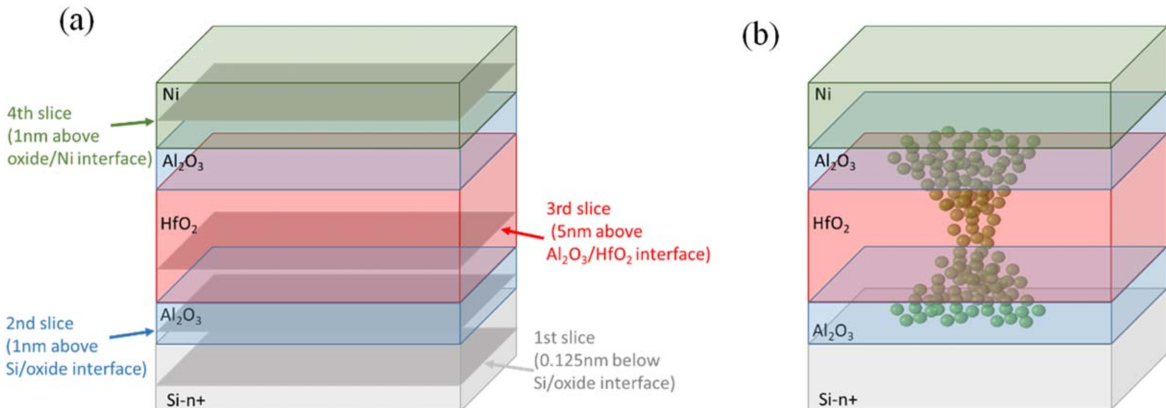


Figure 12. (a) Simulation domain of the device under study. The dielectric trilayer ($Al_2O_3/HfO_2/Al_2O_3$) stack and electrodes are included; the simulations were performed for the DS4 and DS5 structures. The four slices where the temperature distributions in the cross-sections are considered for the analysis are also indicated. (b) Device structure with a symmetric truncated-cone-shaped CF, as used in the simulation scheme.

example, figure 8 shows the *I–V* curves of the forming step and the 2000 RS cycles for the $Al_2O_3/HfO_2/Al_2O_3$ DS, where characteristic RS parameters such as voltages at which forming, set and reset processes occur, $V_{FORMING}$, V_{SET} and V_{RESET}, respectively, and the currents at the HRS and LRS are indicated.

To perform a statistical analysis, the aforementioned parameters were extracted from the 2000 RS cycle measurements for each DS. Figure 9 shows the experimental cumulative distribution functions (CDF) of the HRS and LRS current values, measured at -0.5 V. In the HRS case, the CDF of HfO_2 (red curve) and HfO_2/Al_2O_3 (brown curve) are shifted to slightly larger and lower current values, respectively, in comparison with the other stacks whose CDFs are overlapped. However, in the LRS case, no correlation between the CDF curve and the DS is found. Focusing on curve spreads, similar cycle-to-cycle variability is observed for the different DS for both, HRS and LRS currents. However, larger variability is observed in HRS with respect to LRS. This larger variability is attributed to the variation of the gap distance in the filamentary path after each reset process.

Figure 10 shows CDFs of the extracted set and reset voltages (V_{SET}, V_{RESET}). For both voltages, a similar variability is observed for the different DS combinations. However, whereas an overlapping of V_{SET} CDF curves is observed, two different clear trends can be noticed in the case of the V_{RESET} CDF curves. First, the HfO_2 (red curve) and $Al_2O_3/HfO_2/Al_2O_3$ (soft blue curve) stacks show lower values than the other stacks, with reset voltage distributions shifted ~ -0.5 V. In addition, the CDFs of the current values at V_{SET} and V_{RESET}, I_{SET} and I_{RESET}, respectively, are depicted in figure 11. It is remarkable that CDF curves of I_{RESET} values clearly overlap for all DS while I_{SET} CDF curves slightly differ among each other, being the stack with a single HfO_2 (red curve) layer the one with the largest values of I_{SET}. Notice that for the single HfO_2, the HRS current is also slightly larger (see figure 9).

From this study, we can conclude that although the order and number of layers of HfO_2/Al_2O_3 multilayer stacks strongly influences their electrical properties, in terms of RS performance the main parameter that shows a clear dependence between the different HfO_2/Al_2O_3 multilayers stack combinations is the reset voltage. In order to shed some light on this issue thermal simulations are presented in the next section.

4.2. Analysis of the temperature distributions along CF

Focusing on the results obtained in figure 10, where the reset distribution of HfO_2 and $Al_2O_3/HfO_2/Al_2O_3$ stacks are shifted ~ -0.5 V from the rest of stacks, the impact of the DS on the reset voltage is studied using a simulation tool that solves the 3D heat equation [33–35]. This numerical procedure is in line with other works related to the study of thermal effects in RRAM devices [36–39]. Previously published results [34], showed that Ni-based devices with a single layer of aluminum oxide had higher reset voltages and lower temperature distributions than a single HfO_2 layer or HfO_2/Al_2O_3 bilayers. This result is linked to the higher thermal conductivity in Al_2O_3 ($k_{th} = 2.86$ W m^{-1} K^{-1}) with respect to HfO_2 ($k_{th} = 1.0$ W m^{-1} K^{-1}). In the first case, the lateral heat flux from the CF to the oxide is higher and in order to achieve the temperature that triggers the reset process, higher Joule heating effects are needed, therefore a higher reset voltage is expected. In this work, devices with trilayer DS $Al_2O_3/HfO_2/Al_2O_3$ and $HfO_2/Al_2O_3/HfO_2$ (figure 10) have been studied in terms of temperature distributions. The devices have been analyzed at the LRS considering that Joule heating occurs in the metallic-like CF, which is formed by Ni atom clusters and modeled with cylindrical and truncated-cone shapes. The simulation tool is described in detail in the supplementary material (available online at stacks.iop.org/NANO/31/135202/mmedia) along with the numerical implementation of the 3D heat equation and the algorithm employed to solve it.

Simulations have been performed assuming a device voltage of -1 V and the current is modeled flowing through a fully formed symmetric truncated-cone shaped CF. After the simulations are performed, different temperature distributions

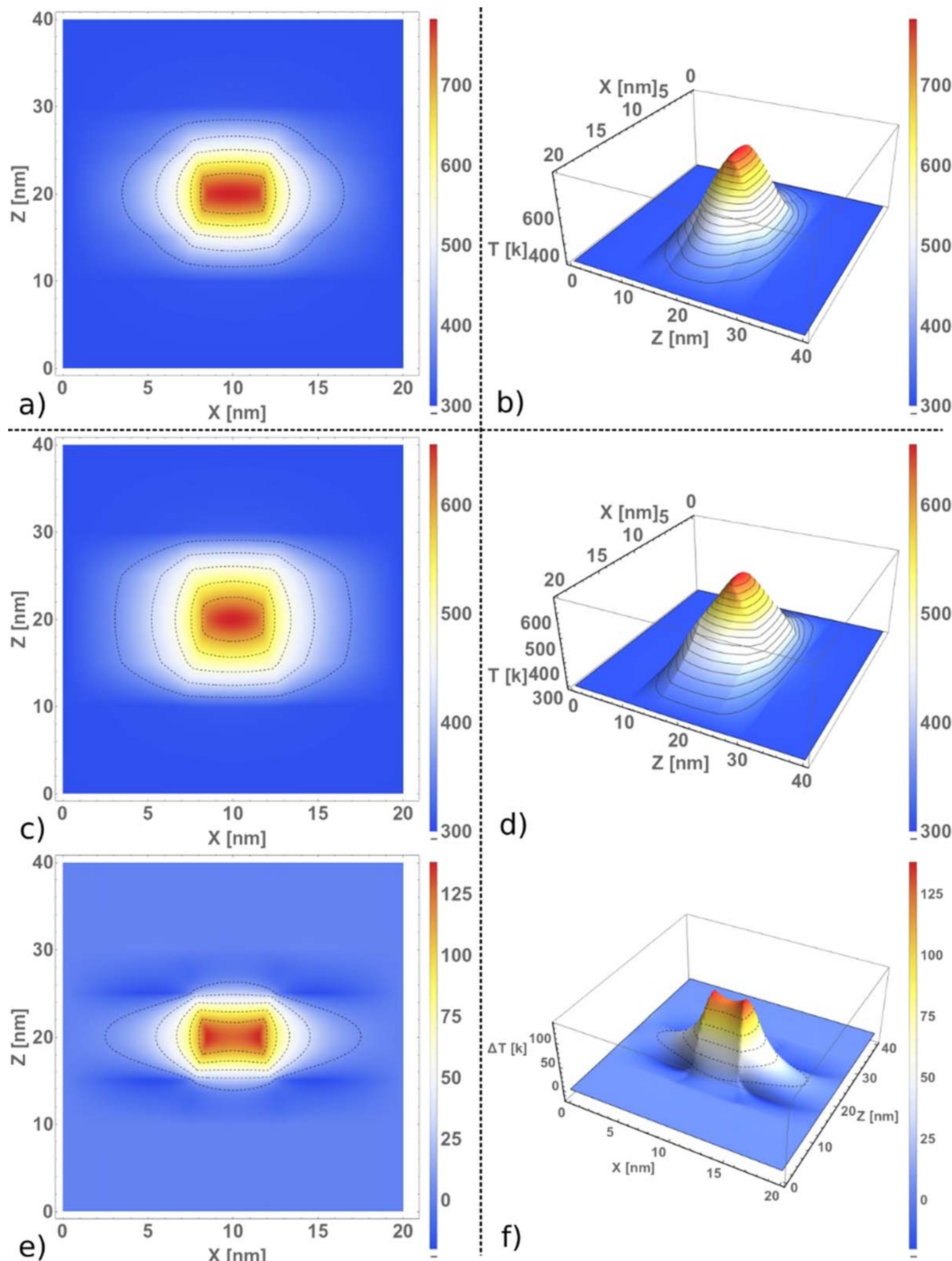


Figure 13. Temperature distribution along the vertical direction (*Z* axis, from the Si to the Ni electrodes) for the devices with $Al_2O_3/HfO_2/Al_2O_3$ (DS4, (a) contour plot, (b) 3D plot) and $HfO_2/Al_2O_3/HfO_2$ (DS5, (c) contour plot, (d) 3D plot) dielectric stacks. The cross-sections were taken at the middle of the *Y* axis, corresponding to the position where the CF revolution axis is found. The electrode layers included in the simulations are also shown (*Z* axis, Si electrode: $0 < z < 10$ nm, and Ni electrode: $30 \text{ nm} < z < 40$ nm). (e) Contour and (f) 3D plots of the subtraction of the temperature distributions shown in (a)–(d).

cross-sections in the 3D simulation domain for the devices under study have been plotted (see the supplementary material). Figure 12(a) shows a sketch of the simulated trilayer DS $Al_2O_3/HfO_2/Al_2O_3$ (in addition to the electrodes) that constitutes the simulation domain (a similar domain is employed in the DS5 case). The slices (cross-sections) employed to study the temperature distributions are located at the different positions figure 12(a). The electrodes are also taken into consideration in the simulation (10 nm in each electrode layer). The simulations were performed accounting for symmetric CFs with their narrow part placed at the dielectric central region (figure 12(b)). This reasoning was in line with a previous study for devices with single and two dielectrics layers [33, 34].

In figure 13, the temperature distributions along the vertical simulation domain axis, from the Si electrode to the Ni electrode, for $Al_2O_3/HfO_2/Al_2O_3$ and $HfO_2/Al_2O_3/HfO_2$ devices are shown. It can be seen that the temperature for the $Al_2O_3/HfO_2/Al_2O_3$ is higher in the central dielectric region, where the CF narrowing is found, as expected taking into account the lower thermal conductivity of HfO_2 with respect to Al_2O_3. Contour and 3D plots are given in this figure (plots (e) and (f) show the temperature difference distribution found between the two types of devices under consideration). The higher temperature in the $Al_2O_3/HfO_2/Al_2O_3$ central dielectric region suggests that the self-accelerated processes linked to RS are triggered in these devices at lower voltages since the structure is thermally more efficient to accumulate the dissipated heat. See also temperatures close to 300 K in the electrodes and in the regions far from the filament, where heat dissipation takes place; this result is coherent from the thermal viewpoint. The simulation results explain, therefore, the experimental results shown above and confirm the influence of temperature on RS mechanisms. The different thermal conduction properties of the materials employed in the DS allow the modulation of the operation temperature within the devices. In doing so, the control of essential operation parameters such as the reset voltage is achieved, facilitating the fabrication of what it could be called thermally engineered devices to lower the power consumption of circuits based on these technologies.

5. Conclusions

MIS devices with bilayer, trilayer and pentalayer DS combining and alternating HfO_2/Al_2O_3 have been fabricated with the aim of studying the impact of the different dielectric configurations on electrical characteristics and the RS performance. The results show larger EOT for HfO_2/Al_2O_3 stacks compared to a single HfO_2 layer, because of the lower Al_2O_3 dielectric constant, and indicate the presence of larger fixed negative charge in the Al_2O_3 layers. Moreover, a larger breakdown strength under both polarities have been observed for multilayer stacks compared to a single HfO_2 layer. The results from RS analysis have shown relevant dissimilarities in V_{RESET} parameters between the fabricated DS combinations. V_{RESET} is shifted ~ -0.5 V for the case of single layer HfO_2 and $Al_2O_3/HfO_2/Al_2O_3$ compared to the rest of the stacks. In order to shed some light into this issue, thermal simulations have been carried out considering that Joule heating occurs in the metallic-like CF. The results reveal that the differences in V_{RESET} values among the stacks could be associated to different temperature distributions at the narrowest part of the CF obtained during the thermally triggered reset process.

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