PAPER

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Photonic crystal based all-optical half adder: a brief analysis

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Abstract

A photonic crystal (PhC) based optical component paves a path to the upcoming all-optical computer processors. All the components can be realized with the help of PhCs. In particular, optical gates have played a major part in the development of all-optical half adders which has lead to the bloom of optical computing technology. In this paper, a PhC based optical half adder is proposed and a brief analysis is carried out for the different crystal structures and lattice patterns. The efficiency of the device is analyzed by providing proper distinct space in output power between logical '0' and '1' states and it operates well even in the reduced input power level. The error can be minimized while identifying the logical states (logic '0' and logic '1'), by setting a threshold limit for output power. The threshold level is fixed such that if it is greater than 0.7 μW, it is considered as logic '1', and if it is less than 0.35 μW, then it will be taken as logic '0'. The device with circular crystals in a hexagonal lattice provides a better contrast ratio of 12.55 dB and 9.29 dB for 'sum' and 'carry' respectively. The miniature size of the proposed device depicts that this device is compatible with photonic integrated circuit (PIC) applications.

Keywords: all-optical XOR gate, all-optical half adder, photonic crystal (PhC), bandgap, electric field distribution, polarization

(Some figures may appear in color only in the online journal)

1. Introduction

In order to overcome the speed limitation and security issues engendered by electronic devices, researchers have found that all-optical communication technology offers the best alternative [1]. In order to make all-optical communication successful, many photonic crystal (PhC) based devices have been designed and developed to fulfill the needs of all-optical communication. A significant challenge to optical computing is nonlinear processing in which multiple signals interact. Light, an electromagnetic wave, can only interact with another electromagnetic wave in the presence of electrons in a material, and the strength of this interaction is much weaker for electromagnetic waves than for the electronic signals in a conventional computer. This may result in the high power and larger dimension processing elements for an optical computer than those for a conventional electronic computer using transistors. It demands the necessity of entire components used in optical networks to be all-optical elements. For telecommunication and data communications, bandwidth is an important criterion that determines the efficiency of the entire system [1]. All the problems faced by the electronic systems are overcome by the elegant features of all-optical communication. Speed in the range of Tbps (terabits per second) can be achieved only when all the electronic components are replaced with optical components [2]. PhCs can be used to design optical components because of various advantages such as low transmission losses,

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increased computational speed, immunity to electromagnetic interference, being free from electrical short circuits, having a large bandwidth, and being capable of communicating several channels in parallel without interference [3]. Also, photonic integrated circuits (PICs) are known to be superior among all other known technology because of their low cross talk, high bandwidth, them having less transmission delay [3] and so on. Components such as splitters, couplers, multiplexer/-demultiplexer, encoders, logic devices, modulators/demodulators, switches, routers, and analog-to-digital converters [4–10] are being designed and reported using PhCs especially for PIC applications. Optical gates play a major part in the development of all-optical half adders which are considered as a key candidate in the fabrication of all-optical computer processors. Logic gates with half adders are designed by using various techniques such as the beam interference method, the self-collimation method, cross structures, two-dimensional (2D) method, and T-shaped waveguides which were analyzed using simulations [11–14]. A Mach–Zehnder interferometer made of PhC waveguides is reported in which the counter-propagating beams are allowed to pass through the nonlinear waveguide in order to design all-optical NOT and AND gates [15]. The AND gate is designed using a Y-shaped PhC waveguide [16] and also gates with a T-Shaped waveguide [17] were simulated and reported [18]. The low power logic NOT gate is also reported without any optical amplifiers and any nonlinear materials [19]. With the help of this literature, the importance of the optical logic circuit in PIC applications is evidenced. In this paper, an all-optical half adder is proposed with a good split-up capability to classify logic '0' and logic '1' in the output port. The wavelength for the simulation should be in the photonic bandgap (PBG) range in order to limit and conduct the light in defect lines. Thus, the 1550 nm wavelength is chosen for simulating the proposed structure. Along with this, the results for the wavelength range of 1553 nm to 1610 nm are also reported. The bandgap structure, design, and its operation, selection of wavelength, and calculation of contrast ratio are analyzed and explained briefly in the following sections.

2. Conventional half-adder design

The half adder is the simplest structure used for combinational as well as arithmetic logic functions which are mainly used by the arithmetic logic circuit of the computer to compute binary addition operations. Two input bits can be processed to produce two output bits as 'sum' and 'carry'. The truth table for the conventional half adder is shown in table 1. If the inputs A and B are different (i.e. A = 0 and B = 1 or A = 1 and B = 0), the output at the 'sum' port will be logic '1' and for identical cases (i.e. A = B = 0 or A = B = 1), its output will be logic '0'. Similarly, for the 'carry', the output will be logic '1' for a unique case (A = B = 1) and the output will be logic '0' for all other cases. Here, the 'sum' output bit is the most significant bit, and the 'carry' output bit is the least-significant output bit. Conferring to the half-adder truth table, the expression for 'sum' and 'carry' output is given as follows:

Table 1. Truth table of half adder.

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\text{'Sum' 'S' = A XOR B} \tag{1}$$

$$\text{'Carry' 'C' = A AND B} \tag{2}$$

From the above expressions, it is clear that the functionality of the half adder solely depends on XOR and AND logic gates. The schematic diagram of the conventional half adder is shown in figure 1.

3. Design and working principle

The band structure is obtained by the plane wave expansion method. The normalized band structure for the proposed structure is shown in figure 2 and it is obtained for the TE Mode. The calculated band structure illustrates that the main PBG is located in the range of $a/\lambda = 0.29$ to 0.48, such that the wavelength corresponding to this range is 1.3 to 2.13 μm for all shapes such as circle, hexagon and square; the selected wavelength sources should then be in this PBG range and therefore the wavelength range of 1530 nm to 1610 nm is used for this simulation. In this paper, the proposed structure consists of 19 × 19 arrays of 2D PhC silicon dielectric rods ($n = 3.46$) which are implanted in the air substrate of the refractive index ($n = 1$) in a triangular lattice pattern like a fused coupler with waveguides. In this structure, the defects are created by eliminating the corresponding PhC dielectric rods in its structure. Silica rods with a refractive index of 3.46 and dielectric constant 'ε_r' of 11.56 are used for this design [16]. The radius 'r' of the PhC in this work is considered as 0.18 a, where 'a' is the lattice constant, a distance between the two dielectric rods.

Several junction rods and reflection rods are used to optimize the efficiency of the half adder in all the shapes. For the circle shape, the radius of each junction/reflection rod is chosen as 0.09 a so that the half adder results in the optimized output; it is observed that the maximum power is transmitted at the output ports ('sum' and 'carry' outputs). For the hexagonal shape, the shape of the rod is entirely different from the circle and square-shaped rods. The hexagonal-shaped rods have six sides whereas the square has four sides. When compared with a circle-shaped rod, the hexagonal has an equal radius only at the point joining the two sides of the hexagonal faces whereas the circle shaped rod has an equal radius at every point along the circle. For square shape structure, the side of the square

Table 2. Input and output values for the half adder for various shapes at 1550 nm.

Input power = 1.0 μW															
INPUT				OUTPUT											
A		B		Circle				Hexagon				Square			
				S		C		S		C		S		C	
VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC	VALUE	LOGIC
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1.0	1	0.85	1	0.3	0	0.82	1	0.3	0	0.83	1	0.13	0
1.0	1	0	0	0.9	1	0.1	0	1.0	1	0.1	0	0.8	1	0.15	0
1.0	1	1.0	1	0.05	0	0.85	1	0.09	0	0.75	1	0.1	0	0.85	1

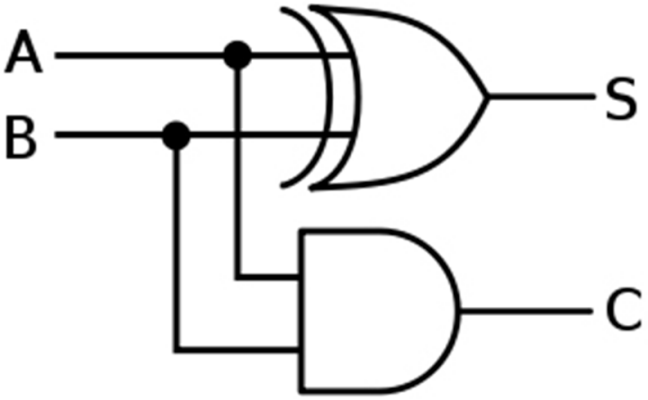


Figure 1. Schematic of conventional binary half adder.

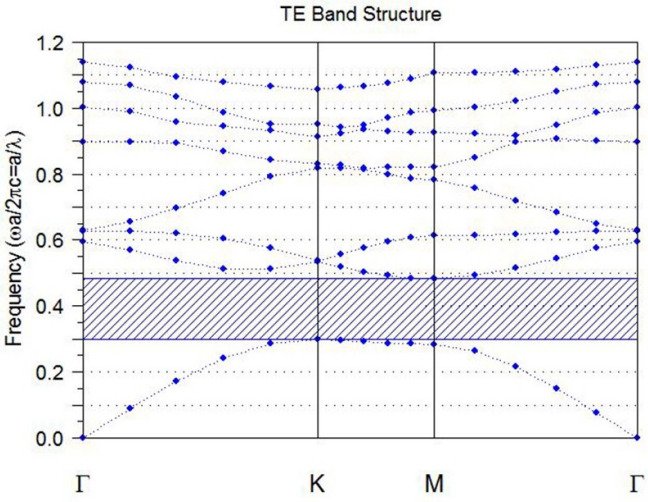


Figure 2. Calculated bandgap for proposed structure.

rods is twice that of the radius of the circle rods due to the difference in its structure from the square and circle in turn. However, the radius is referred to as having half the distance of the side of the square-shaped rod. Figures 3(a)–(c) show the layout of the all-optical half-adder design and it is simulated using a finite difference time domain method.

4. Results and discussion

The proposed all-optical half adder has two inputs (A and B) and two outputs (S and C), where S is the 'sum' output bit and C is the 'carry' output bit. Two optical sources 'A' and 'B' with the corresponding wavelength are used as inputs. The defect lines are created by either adding/removing rods or varying the radius of the rods. The defect lines of the inputs and outputs of the proposed half adder are shown in the layout (figures 3(a)–(c)). The defect lines are selected to intercross each other such that they couple the incoming sources and split to the outgoing port. The radius of the five scatter (blue-colored) rods in the center of the layout is condensed to '0.5 r', where 'r' is the radius of base (red-colored) rods. These rods act as scatters which are used to control and conduct the electric field in their output ports.

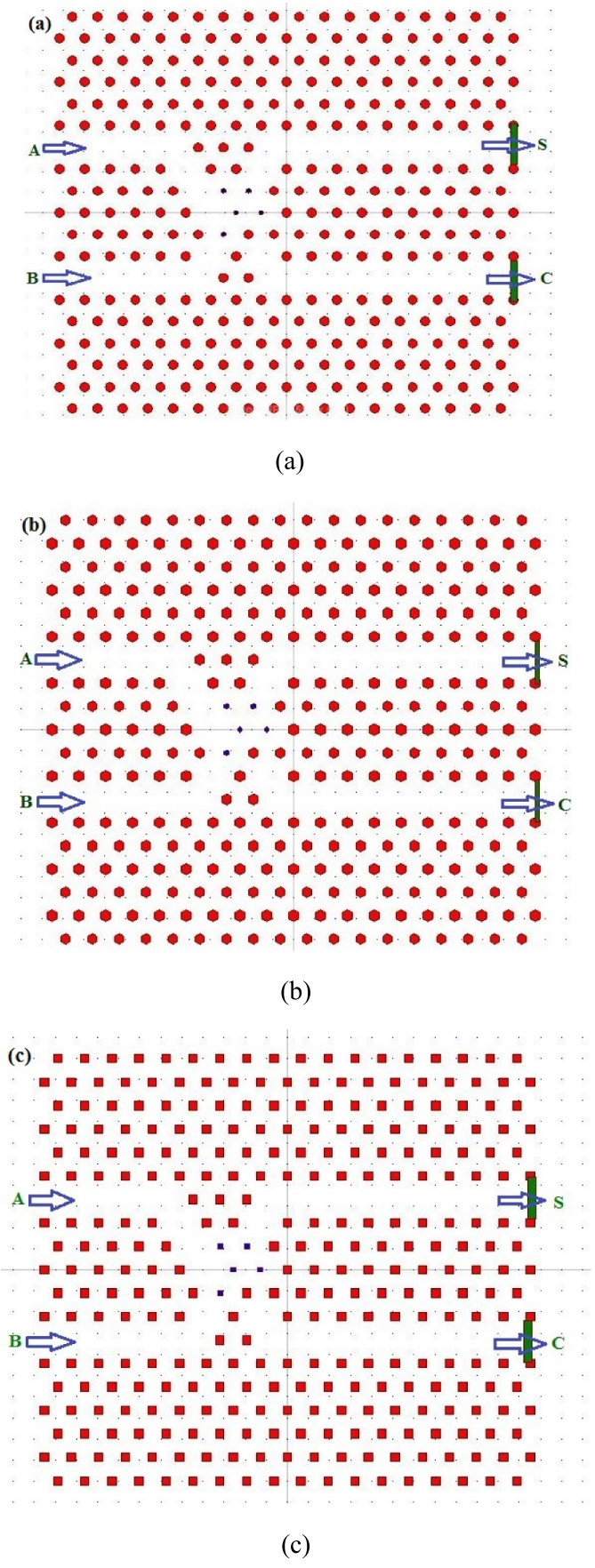
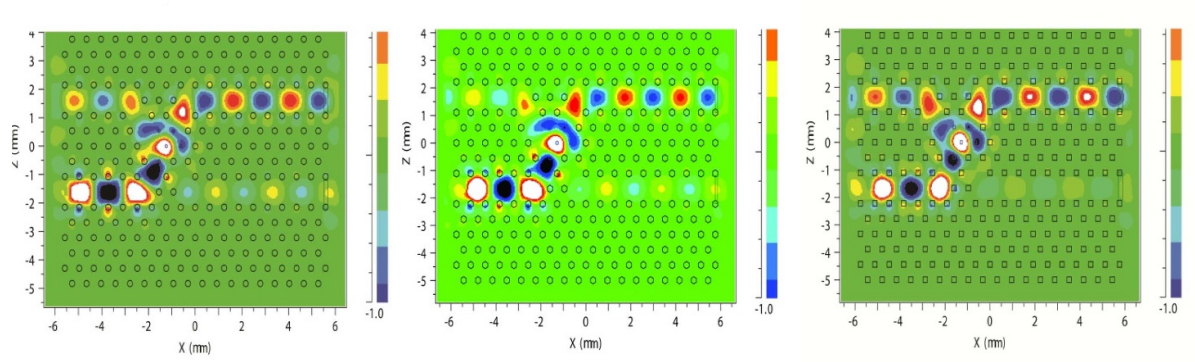
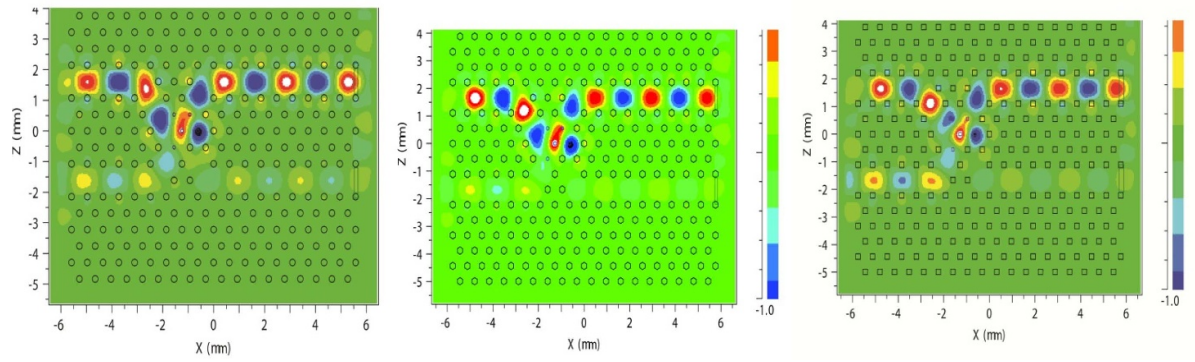


Figure 3. Layout design for half adder: (a) circle (b) hexagon (c) square.



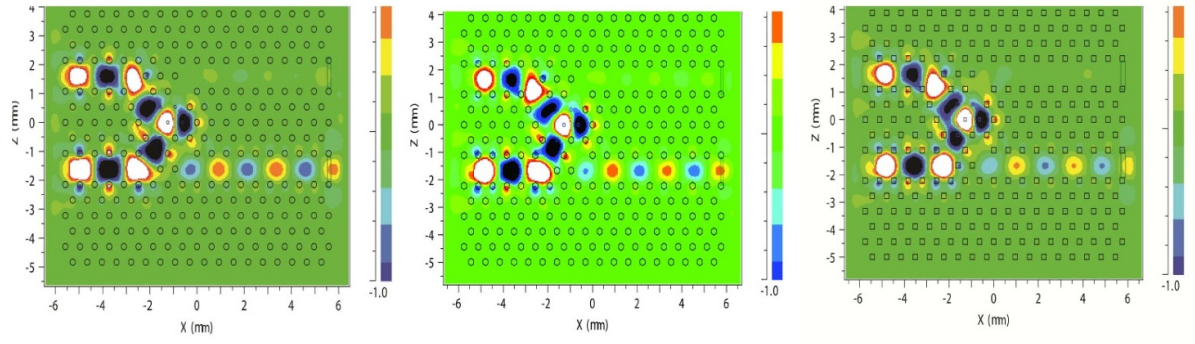
(a) (b) (c)

Figure 4. Electric-field distribution of the inputs A = 0, B = 1 for (a) circle (b) hexagon (c) square.



(a) (b) (c)

Figure 5. Electric-field distribution of the inputs A = 1, B = 0 for (a) circle (b) hexagon (c) square.



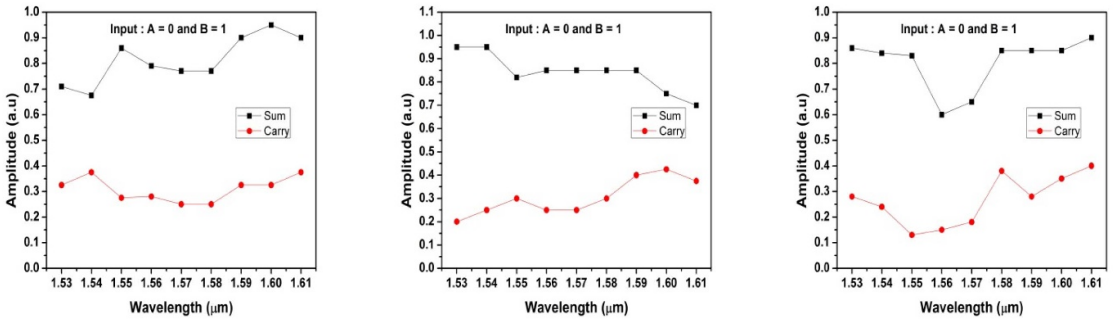
(a) (b) (c)

Figure 6. Electric-field distribution of the inputs A = 1, B = 1 for (a) circle (b) hexagon (c) square.

Case (i): A = B = 0. In this case, there is no input permissible to pass through this structure, hence the output will be logic '0' for both 'sum' and 'carry' output port.

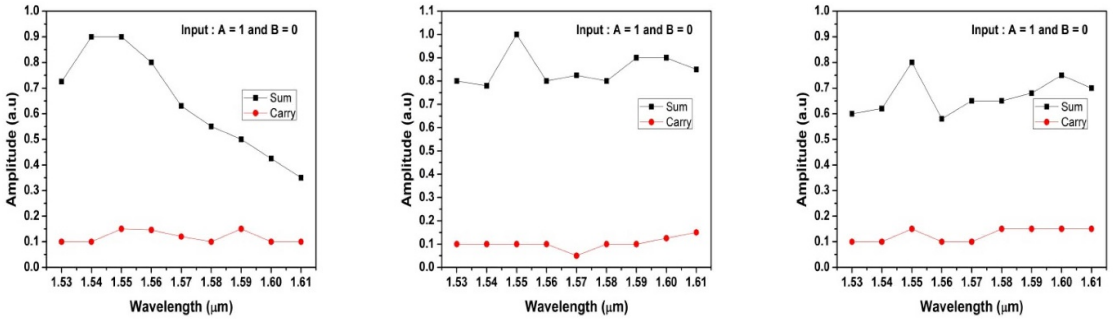
Case (ii): A = 0, B = 1. For this case, the outputs obtained for the circle, hexagon and square shape are given in figures 4(a)–(c), respectively. When one of the inputs is LOW, logic '0', and the other is HIGH, logic '1' (i.e. A = 0 and B = 1 or A = 1 and B = 0), then the electric field in output 'S' will be substantial such that it is equal to logic '1'. However, the output 'C' will have a low electric field which is equal to logic '0'. This case for all three shapes is shown in figure 4.

Case (iii) A = 1, B = 0. While in this case, one of the inputs says that 'A' is HIGH, logic '1', and the other input says that 'B' is LOW, logic '0', then the output will remain the same as for the above case. The 'sum' output will be HIGH, logic '1', whereas the 'carry' output is LOW, logic '0'. This case is clearly shown in figures 5(a)–(c) for the circle, hexagon, and square shape of the half adder.



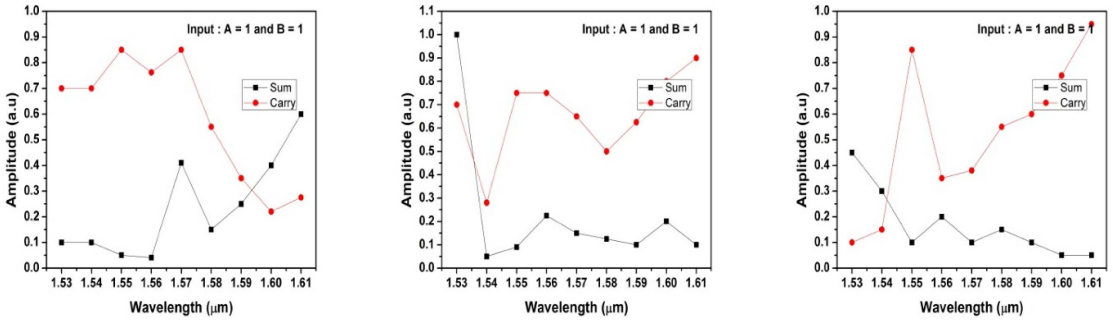
(a) (b) (c)

Figure 7. Output graph for various wavelengths with inputs A = 0 and B = 1 for (a) circle (b) hexagon (c) square.



(a) (b) (c)

Figure 8. Output graph for various wavelengths with inputs A = 1 and B = 0 for (a) circle (b) hexagon (c) square.



(a) (b) (c)

Figure 9. Output graph for various wavelengths with inputs A = 1 and B = 1 for (a) circle (b) hexagon (c) square.

Case (iv) A = B = 1. When A = B = 1, the condition at the output ports will be reversal of all other cases such that the electric field distribution in 'sum' output port 'S' is very LOW in order to represent the logic '0' state; furthermore, in the 'carry' output port 'C' is HIGH in order to represent the logic '1' state. This case is described well in figures 6(a)–(c) for every shape of the half adder. The input and output values for half adder for different shapes at 1550 nm are listed in table 2.

In this simulation, the variation in the electric field for various input values for various shapes is calculated for the entire C-band wavelength ranges (1530 nm to 1610 nm). There is possibly a reflection of light or flow of light i.e. the electric field in the undesired output that maybe results in path loss

Table 3. Comparisons of proposed work with various shapes.

Rod Shape	Contrast Ratio (dB)	
	Sum	Carry
Circle	**12.55**	**9.29**
Hexagon	10.45	8.75
Square	9.19	7.53

Table 4. Comparisons of proposed work with existing results.

Authors	Input Power Level	Output Power Ranges (μW)		Contrast Ratio (dB)	
		Logic '0'	Logic '1'	'Sum'	'Carry'
M Ghadrdan and M A Mansouri-Birjandi 11]	277 mW	<0.3	>0.7	5.6	12.7
Q Liu *et al* [14]	274 mW	<0.1	>0.2	16.47	23.92
M M Karkhanehchi *et al* [13].	1.4 μW	<0.4	>0.6	6.11	3.52
Our Proposed Work (Circle)	1.0 μW	<0.35	>0.7	12.55	9.29

which leads to some of the minority fields in the undesired output port and is considered as logic '0'. Also, because of path losses of the electric field, the output that appeared in the output port of 'sum', and 'carry' does not achieve its level as equal to input power; still, it it considered as logic '1'. There is an asymmetry between the inputs at the junction which leads to the desired output. For the A = B = 0 case, there is no need for input power; it is just in the 'OFF' stage, so that the output in 'sum' and 'carry' is exactly zero. For A = 0, B = 1 and A = 1, B = 0 of unequal inputs, the output that appeared at the 'sum' port of both cases is found to be HIGH and it is almost nearer to the given input power (figures 7 and 8), whereas, in the 'carry' port, the output signal seems to be LOW which is nearer to zero. At the terminal case, for A = B = 1 inputs, the output at 'carry' seems to be HIGH; higher than the 'sum' output which is shown in figure 9. In order to contract the error detection, two novel terms are used—the upper threshold (UT) level and lower threshold (LT) level. These levels are fixed with 0.7 μW as the UT level and 0.35 μW as a the LT level.

It is clearly understood that the device works well in the wavelength of 1550 nm from the figures 7, 8, and 9. Even the output for any one of the cases (either 'sum' or 'carry'), is higher than the UT level; a much higher level is not considered. This is purely based on the distinct spacing between the peak of the 'sum' and 'carry' output level for a particular wavelength. Further, it is proven that in the source wavelength of 1550 nm, the 'sum' output satisfies the UT level and the 'carry' output satisfies the LT level condition, also providing a better distinct level than the outputs with other wavelengths. The comparison among the various shapes of the device is performed internally by its contrast ratios and the best results with this structure are then compared with other literature in terms of its power level, contrast ratio, and threshold logic levels. By performing these comparisons, the advantages behind this structure are proved and suggest optical processing applications for the future.

5. Contrast ratio

Contrast ratio is defined as the ratio of 'ON' power to the 'OFF' power. It is given by the following relation [11].

$$\text{CR} = 10 \log \text{PON/P'OFF'} \tag{3}$$

where, 'P_{ON}' and 'P_{OFF}' are the output power levels of logic '1' and logic '0', respectively. The contrast ratio of 'sum' and 'carry' is about 12.55 dB and 9.29 dB for the circle, 10.45 dB and 8.75 dB for the hexagon, and 9.19 dB and 7.53 dB for the square, respectively. Thus the improved contrast ratio obtained for circle-shaped rods provides the widespread role in PIC applications. The salient advent of the proposed PhC half adder is compared with the structure itself and also with other existing literature and tabulated in tables 3 and 4 respectively.

From tables 3 and 4, it is noticeable that the proposed structure has a better contrast ratio for circle-shaped rods than other structures and also it is a satisfying work when compared with the other literature work; furthermore, it also offers appropriate distinct space in its output power between '0' and '1' logical states.

6. Conclusion

A PhC based all-optical half adder for the PIC is deliberated and its output is evaluated in terms of output 'sum' and 'carry'. The results for all four combinations of inputs are studied. For a) A = 0, B = 1, b) A = 1, B = 0 c) A = B = 1 cases, the obtained output power level for 'sum' and 'carry' are with various power levels for various shapes. The comparison is made with all those shapes and it is found that circle-shaped rods provide better results than other structures. The better result of the circle shape of the rods is then compared with other existing designs. However with the lesser input power level of about 1 μW, there exist better distinct output power levels for logic

'0' and logic '1'. Improvement in the contrast ratio (12.55 dB for 'sum' and 9.29 dB for 'carry') and ultra-compatibility has also proved that this proposed compact design can be certainly used for a PIC.

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