Modular Multilevel Converter Based Topology for High-Speed, Low-Voltage Electric Drives

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***Abstract*—The increasing demand for higher power density and more efficient electric drives, in particular, from the automotive industry, has pushed engineers investigating new solutions. Recently, wide bandgap devices have been proposed to improve performances of classical ac/dc converters, mainly in terms of power conversion efficiency. In this article, an alternative approach is proposed, aiming to obtain the desired improvements in the overall drive performances using a more complex power conversion system, based on standard silicon devices. In particular, a modification of the modular multilevel converter (MMC) is proposed in order to eliminate the submodule voltage ripple that would otherwise limit the MMC applicability in low voltage, variable frequency electric drives. This article introduces the design procedure and the analytical modeling of this novel topology together with the validation of the theoretical claims via simulations and experimental tests.**

***Index Terms*—Dual active bridge, modular multilevel converter (MMC), power electronics.**

I. Introduction

THE increasing demand of electric vehicle (EV) from the automotive industry is leading research toward higher power density and more efficient electric drives [1]. Automotive drives feature several electrical machines (EMs) and power electronic converters (PECs) that control speed and torque produced by the EM, manage the batteries state of charge (SOC) whilst maintaining a high overall efficiency [2]. Regarding the EM design, important technological improvements have been obtained during the last 15 years, with noticeable improvements in peak power, peak power density, and peak specific power [1]. The EM design is usually strictly coupled with the PECs that are considered for the application. Traditionally, two-level bidirectional ac/dc and dc/dc converters are considered. For example, Fig. 1 shows a classical drive structure, where one 2-level inverter is used to drive the electric motor, one 2-level rectifier control the dc-link bus during regenerative braking and one bidirectional dc/dc converter controls the battery SOC and vary the value of the dc-link during transients [1].

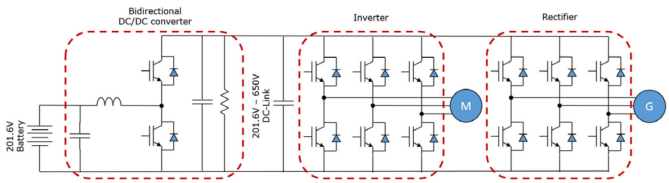

Fig. 1. Example of automotive electric drive [1].

As for the EM, technological achievements are noticeable in the power electronics. Improvements in power density and specific power can be noted and are mainly achieved by the adoption of more performing semiconductors and optimized integrations of the PECs. [3]. The continuing demand for high efficiency, more compact and cost-effective drivetrains will further push the electric drive designers to achieve higher efficiency whilst reducing the mass, volume, and cost [3]. An additional drive to improve the PEC performances comes from the EM designers. EMs with a high number of pole pairs have been investigated in order to improve the power density and efficiency [4], [5]. This leads to higher fundamental frequencies to be controlled by the PEC and, as a consequence, faster switching [1], [6].

A solution to improve the PECs efficiency and be able to control high fundamental frequencies is to take advantage of multilevel converter topologies [7]–[10]. In fact, multilevel converter aims to improve the PECs performances by replacing the two-level inverter and rectifier of Fig. 1 with a more complex topology using standard Silicon devices [11]–[14]. The main advantages of multilevel converter topologies over standard two-level converters are reduced losses, high output switching frequency, modularity, and fault tolerance. In fact, multilevel converters enable the use of lower voltage rated devices, resulting in lower switching and conduction losses and increased efficiency [14] whilst obtaining an output switching frequency that is multiple of the single device switching frequency, allowing the control of high fundamental waveforms. Moreover, many multilevel converter topologies present a modular structure, with identical cells connected in series and parallel. This feature eases the converter design and scalability, as well as enabling fault

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tolerance capabilities. The main disadvantage of the multilevel converter is the increased number of components and, thus, lower power density with respect to simpler topologies. However, this issue can be addressed by an optimized converter design for the specific application [13]. Another important drawback of multilevel converters with respect to the simpler two-level topologies is its control complexity [7], [8], [15]. This, depending on the multilevel converter topology under investigation, may require additional measurements and control algorithms that perform essential tasks for enduring the converter controllability. For example, in several modular multilevel topologies it is necessary to balance the dc voltage of the single modules, in order to maintain symmetrical output waveforms [14], [16], [17]. Focusing on modular structures, Cascaded H-Bridge (CHB) converters feature several H-Bridge cells connected in series, in order to obtain multilevel waveforms [18], [19]. For this reason, this specific topology is often proposed for EV traction applications [20]. On the other hand, the main disadvantage of CHB converters when applied to EV is the requirement for galvanically isolated dc ports on each cell. This can be addressed by segmenting the battery pack over the converter cells [21]. However, more complex control is required to guarantee even utilization of each battery segment. Alternatively, a two-stage structure, with an isolated dc/dc converter interfacing the battery pack is required, increasing the number of devices, losses, and converter complexity [22].

A multilevel converter topology, which is less considered in EV applications, is the modular multilevel converters (MMC). The MMC presents numerous advantages with respect to other multilevel converter topologies, in terms of efficiency, modularity, and scalability [23]–[26]. MMC and derived chain-link topologies have recently become the standard in new voltage source HVdc installations and are often considered for medium voltage drives and grids for their low *dv*/*dt*, superior harmonic performance, use of cost-effective low-voltage semiconductors, input and output filter size reduction, high-efficiency and low common-mode voltage. These features make this topology attractive even for low-voltage EV applications. However, one of the main drawbacks of the MMC is that each submodule (SM) handles a power ripple with components at fundamental frequency and twice the fundamental frequency [24]. As a result, the required SM capacitance for a given SM voltage ripple is inversely proportional to the fundamental frequency of the converter. This leads to a relatively large value of capacitance, which in grid applications provides a useful energy storage to ride through abnormal grid conditions but at the same time reduces power density [24]. Techniques have been proposed to reduce the capacitors by altering the circulating currents between the phase arms [27]–[30], but the achievable capacitance reduction is always limited. Other options consider specific control and modulation at low speed, in order to minimize the capacitance value by designing its value at the nominal fundamental frequency, usually higher than 500 Hz [31], [32]. However, these techniques provide additional harmonic distortions or require the variation of the dc-link voltage. Moreover, their application is limited to startup operations. Finally, hardware modification in the MMC structure [33]–[35] have been proposed. However, these techniques result in additional measurements and control complexity, which is not desirable in EV applications where cost and volume are important factors.

This article proposes a hardware modification of an MMC to enable this technology for low-voltage, high-speed drives, as it can be an EV traction system. A similar approach is proposed in [35]–[37]. However, the implementation and control derivation, as well as the converter design, completely differs from those which are proposed in previous works. In fact, the proposed topology is specifically designed for low voltage drive applications, aiming to maintain the control complexity and general features of a two-level inverter. This means first to feature a simplified control system that considers only measurements at the converter terminals, avoiding cell voltage measurements and related capacitor voltage balancing algorithms. Moreover, the proposed topology must present a reduced SM capacitance, aiming to achieve specific power values of the same magnitude order of a Silicon Carbide two-level voltage source inverter. In fact, even if it is clear that the increased number of devices present in such topology may increase the converter volume, it is still possible to obtain a higher power density drive system by considering a specific, high fundamental frequency, EM design [4], [5]. In fact, the main benefit of this topology is to maintain high output switching frequency and, thus, control of higher fundamental frequencies, without the need of using wide bandgap (WBG) devices, such as SiC. Indeed, due to their well-known reliability and low *dv*/*dt* (i.e., lower EMI), Silicon devices are often preferred in automotive applications [6]. At the same time, the proposed topology must provide high-efficiency power conversion, taking advantage of high-performance low-voltage, high-current MOSFETs.

The article is organized as follows: in Section II, the proposed topology is described in detail, starting from the single SM ac analysis and dual active bridge (DAB) operations. Additionally, the converter design is described in detail. Simulation and experimental results are provided in Sections III and IV, respectively, in order to validate the feasibility and performance of the proposed converter topology. In Section V, conclusion is put forward and further work is discussed.

II. Description of the Topology Under Study

A single phase of the proposed topology is shown in Fig. 2. It comprises the classical MMC arm structure based on half-bridge SMs with the addition of dual active-bridge coupling converters [38]. In terms of principle, the proposed topology operates as a classical MMC, with the DAB converters presenting an independent open-loop control.

When the classical MMC switching patterns are considered, there are always an equal number of capacitors connected and bypassed between upper and lower arms. This means that, independent of the output voltage level that is generated by the converter, the number of capacitors charging in the upper arm and discharging in the lower arm is always equal and vice-versa. By enabling a controlled power transfer between upper and lower arm, using the DAB converters, it is possible to maintain the capacitors linked by each DABs at constant and

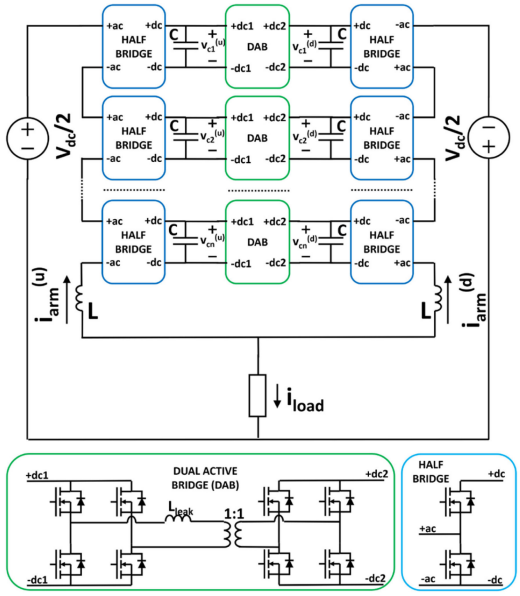


Fig. 2. MMC topology under consideration.

equal voltage levels, even when values of capacitance in the order of microfarad are considered. The half-bridge cells are modulated using phase-shifted carrier (PSC) modulation [39] whilst the dual active bridge is modulated using single-phase shift (SPS) modulation [40]–[43]. PSC has been selected for the H-bridge modulation for its clear advantages in simplifying the control structure. In fact, the SM capacitor voltage balancing can be achieved naturally using this modulation, by taking advantage of the PSC modulation properties [39] which inherently impose an equal number of commutations for each SM. The modulation is achieved by phase shifting the carrier of $T_{\rm sw}/N$, where $T_{\rm sw} = 1/f_{\rm sw}$ is the commutation period at a switching frequency $f_{\rm sw}$ and N is the number of SMs [39].

In order to further simplify the control system, the DABs are operated in open loop, with the power transferred by the DAB, necessary to achieve capacitors voltage ripple cancellation, calculated directly from iarm(u), iarm(d), as shown later in the topology description. These features also allow avoiding the SM capacitors voltage measurement, thus reducing the converter size and complexity. With this consideration about the DABs operation in mind, SPS modulation has been selected. SPS is the simplest DAB modulation techniques. The two H-bridges generate symmetrical square waveforms, with 50% of the duty cycle. The power transfer is controlled by the phase shift between the two square waves. Using this modulation, an analytical expression of the phase shift can be obtained and is used to implement the DABs open-loop control. Moreover, SPS allows soft-switching commutation on devices turned ON, resulting in lower losses and allowing high switching frequency to be selected for DAB operations [42], [43].

A. *Modified MMC Operations*

In order to understand the operating principle of the topology, a simplified converter structure with one SM per arm is considered, as shown in Fig. 3 where the DAB is replaced with an ideal 1:1 transformer. It is important to highlight that the ideal transformer does not represent the DAB model, which is described in Section II-b, but only the idealized operating condition in which the DAB converter is able to achieve zero voltage ripple on the two SM capacitors. From the model in Fig. 3, the load current can be directly derived by the arms currents as follows:

$$i_{\rm load} = -\left[i_{\rm arm}^{(u)} + i_{\rm arm}^{(d)}\right]. \tag{1}$$

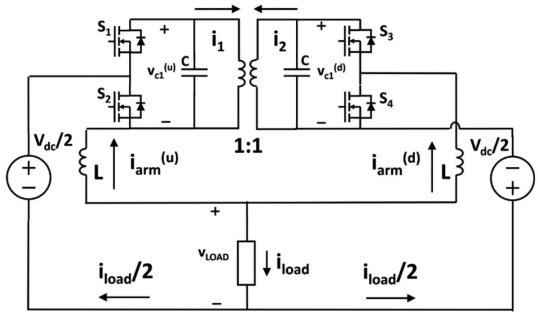


Fig. 3. MMC topology under consideration: simplified converter structure with one cell per arm.

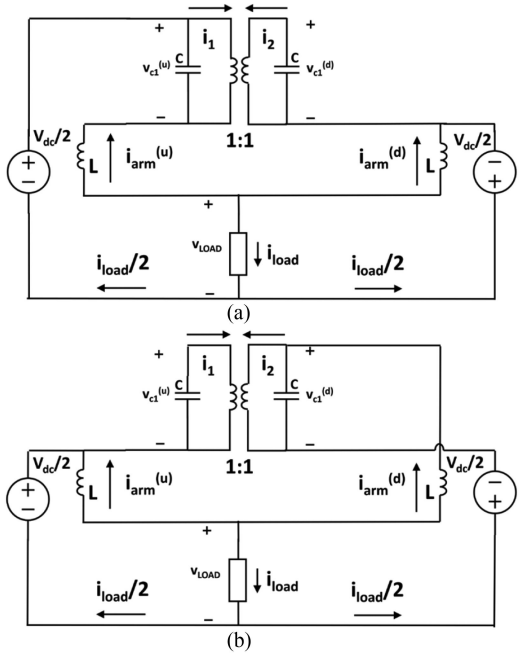


Fig. 4. MMC topology under consideration: switching configurations for the simplified converter structure with one cell per arm.

In order to fulfill the MMC switching rules, that always force one SM in the upper and lower arm to have opposite switching state, only two possible switch configurations are allowed, as shown in Fig. 4.

The first switching state is shown in Fig. 4(a) and corresponds to S_1, S_4 switches turned ON and switches S_2, S_3 turned OFF. In this case, i_1 and i_2 can be expressed

as follows:

$$i_1 = -C\frac{dv_{c1}^{(u)}}{dt}$$
$$i_2 = i_{\text{arm}}^{(d)} - C\frac{dv_{c1}^{(d)}}{dt}. \tag{2}$$

At the same time, the voltage produced on the load is equal to

$$v_{\text{load}} = v_{c1}^{(d)} \simeq \frac{V_{\text{DC}}}{2}. \tag{3}$$

From (1) and (2), it is possible to obtain the converter switching model, considering the state $s = 1$ when S_2, S_3 switches are turned ON and switches S_1, S_4 are turned OFF

$$i_1 = (1-s)\frac{i_{\text{LOAD}}}{2} - C\frac{dv_{c1}^{(u)}}{dt}$$
$$i_2 = si_{\text{arm}}^{(d)} - C\frac{dv_{c1}^{(d)}}{dt}. \tag{4}$$

By considering the load current is imposed by the system, and that the ideal transformer imposes the following constraints to be satisfied:

$$-i_1 = i_2 = i$$
$$v_{c1}^{(u)} = v_{c1}^{(d)} = v_{c1} \tag{5}$$

it is possible to obtain the following model:

$$i = -(1-s)\frac{i_{\text{LOAD}}}{2} + C\frac{dv_{c1}}{dx}$$
$$i = si_{\text{arm}}^{(d)} - C\frac{dv_{c1}}{dx}. \tag{6}$$

By summing the two equations in (6) and considering a modulation index m instead of the instantaneous switching state s, the following expression of the current i can be obtained:

$$2i = -(1-m)\frac{i_{\text{LOAD}}}{2} + C\frac{dv_{c1}}{dx} + mi_{\text{arm}}^{(d)} - C\frac{dv_{c1}}{dx}. \tag{7}$$

By substituting (1) into (7)

$$2i = (1-m)\frac{i_{arm}^{(u)} + i_{arm}^{(d)}}{2} + mi_{arm}^{(d)} \tag{8}$$

it is possible to obtain an expression for i that depends only on the modulation index and the arm currents

$$i = \frac{1}{4}\left[\left(i_{\text{arm}}^{(u)} + i_{\text{arm}}^{(d)}\right) + m\left(i_{\text{arm}}^{(d)} - i_{\text{arm}}^{(u)}\right)\right]. \tag{9}$$

Equation (9) gives an expression for the current that must flow through the isolation stage that links upper and lower cell, in order to equalize the voltages on the two capacitors. This expression is scalable to converters with a higher number of SMs, with the same current flowing through each SM. Clearly, in practical operations, an ideal transformer cannot be considered and has to be replaced by an isolated, bidirectional dc/dc converter. In this case, the DAB converter has been selected for this task.

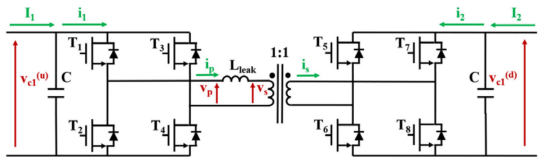


Fig. 5. DAB converter schematics.

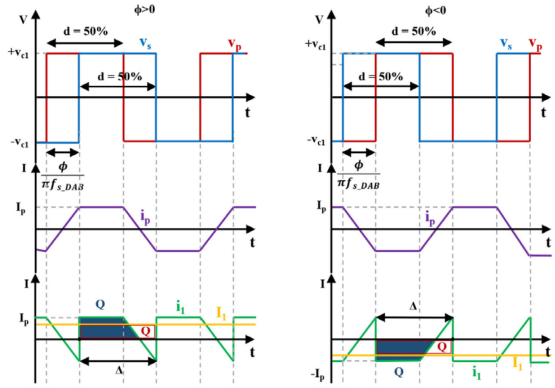


Fig. 6. SPS waveforms for the DAB converter with 1:1 transformer turn ratio.

B. DAB Converter Operations

The DAB converter, shown in Fig. 5, is a well-known topology, which provides efficient dc/dc conversion as well as galvanic insulation. As shown in Fig. 5, the DAB consists of two H-bridge linked on their ac sides with a series inductor and an HF transformer. When SPS modulation is considered, the duty cycle of each H-bridge is kept constant at 50% of the sampling period, while the phase shift φ between the transformer primary and secondary voltage waveform is used to control the power transfer. Theoretical operation waveforms for such topology is drawn in Fig. 6 under the specific constraints expressed by (4), where v_p and v_s are transformer primary and secondary voltages, i_p is transformer primary current. i_1 and I_1 are the currents flowing before and after being filtered by the output capacitor C.

Under these conditions, the power managed by the DAB converter can be expressed as follows:

$$P_{\text{DAB}} = v_{c1}i \tag{10}$$

where i is the current calculated by (9). Considering that the maximum power that can flow through the DAB converter depends on the transformer leakage inductance

$$P_{\text{DAB}}^{\max} = \frac{2v_{c1}^2}{8f_{\text{sw}}^{\text{DAB}}L_{\text{leak}}} \tag{11}$$

it is possible to determine the value of phase shift ϕ to apply as follows [42]–[44]:

$$\phi = \pi\left[1 - \sqrt{\frac{|P_{\text{DAB}}|}{P_{\text{DAB}}^{\max}}}\right]\text{sign}\left(P_{\text{DAB}}\right)$$
$$= \pi\left[1 - \sqrt{\frac{v_{c1}\,|i|}{P_{\text{DAB}}^{\max}}}\right]\text{sign}\left(i\right). \tag{12}$$

From (9) to (12), it can be noted that each DAB manages a power that depends on the arm currents, which are related with the load current i_{LOAD}, the SM capacitance C, and arm inductors values L. In this specific application, the DAB in each SM transfer a power that is a fraction of the output power and its value is strictly related with the chosen design parameters as well as the number of SMs. For the aforementioned reasons, all the DABs in the same converter phase leg share the same driving signal, thus, simplifying the overall system design. It is also important to highlight that (12) is used to emulate the behavior of the 1:1 ideal transformer in Section II-A by imposing a current flowing through the DAB equal to the current i, defined in (9).

C. Overall Converter Design

The power transfer inductance L_{leak} is designed in order to achieve the required power rating for the converter [44]

$$L_{\mathrm{leak}} = \frac{2v_{c1}^2}{8f_{\mathrm{sw}}^{\mathrm{DAB}} P_{\mathrm{DAB}}^{\max}}. \tag{13}$$

In order to design the filter capacitors, the load current at nominal power is calculated from (10) and (13)

$$I_1 = \frac{2v_{c1}}{8f_{\mathrm{sw}}^{\mathrm{DAB}} L_{\mathrm{leak}}}. \tag{14}$$

Referring to Fig. 6, the time interval Δ is equal to half of the sampling period and the area Q can be calculated as follows:

$$Q = \frac{1}{2f_{\mathrm{sw}}^{\mathrm{DAB}}} I_1 = \frac{v_{c1}}{8f_{\mathrm{sw}}^{\mathrm{DAB}^2} L_{\mathrm{leak}}}. \tag{15}$$

Therefore, the normalized peak-to-peak output voltage ripple r_v^{DAB}, expressed as a percentage of the nominal capacitor voltage can be obtained based on the following equation:

$$r_v^{\mathrm{DAB}} = \frac{\Delta v_{c1}}{v_{c1}} = \frac{Q}{Cv_{c1}} = \frac{1}{8Cf_{\mathrm{sw}}^{\mathrm{DAB}^2} L_{\mathrm{leak}}}. \tag{16}$$

The output capacitor C can then be derived from (16) as

$$C = \frac{1}{8r_v^{\mathrm{DAB}} f_{\mathrm{sw}}^{\mathrm{DAB}^2} L_{\mathrm{leak}}}. \tag{17}$$

Moreover, since different from standard DAB applications, an ac power reference is imposed, the converter dynamics, which is limited by the transformer leakage inductance value L_{leak}, and the capacitance C have to be taken into account. In particular, the resonance between leakage inductance and capacitance has to be carefully designed in order to be placed between the third harmonic of the fundamental frequency f_{fun} and the minimum between the DAB switching frequency $f_{\mathrm{sw}}^{\mathrm{DAB}}$ and the SM H-bridge switching frequency $f_{\mathrm{sw}}^{\mathrm{HB}}$ [45]

$$3f_{\mathrm{fun}} \ll \frac{1}{2\pi\sqrt{L_{\mathrm{leak}}C}} \ll f_{\mathrm{sw}}^{\mathrm{DAB}}. \tag{18}$$

Another resonance to consider is the resonance between arm inductance and SM capacitance. This resonance has to fulfill the constraint of (19) in order to maintain operation in the whole operative range

$$\frac{1}{2\pi\sqrt{L_{\mathrm{arm}}C}} \gg f_{\mathrm{fun}}. \tag{19}$$

TABLE I
SIMULATION AND EXPERIMENTAL PARAMETERS

Symbol	Quantity	Value	Unit
P	Single Phase Maximum Power	15	[kW]
V_{dc}	DC Link Voltage	600	[V]
C	Cell Capacitance	63	[μF]
L	Arm Inductance	200	[μH]
L_{leak}	DAB Power Transfer inductance	2.2	[μH]
R_{load}	Load Resistance	30	[Ω]
L_{load}	Load Inductance	450	[μH]
f_{sw}^{HB}	HB switching frequency	10	[kHz]
f_{sw}^{DAB}	DAB switching frequency	100	[kHz]
N	Number of Cells per Arm	10	/

Regarding the MMC, the same capacitor C can also be designed, together with the arm inductance value L, in order to absorb part of the voltage ripple at a specified frequency [46]

$$C = \frac{P_{\mathrm{HB}}^{\max}}{4\pi f_{\mathrm{fun}} r_v^{\mathrm{HB}} v_{c1}^2} \tag{20}$$

$$L = \frac{P_{\mathrm{HB}}^{\max}/P_{\mathrm{HB}}^{\mathrm{2nd}}}{16\pi^2 f_{\mathrm{fun}}^2 C} \tag{21}$$

where $P_{\mathrm{HB}}^{\max} = P_{\mathrm{phase}}^{\max}/N$ is the maximum power managed by a single H-bridge, N is the number of SMs per arm, r_v^{HB} is the allowed voltage ripple allowed on the SM capacitance and $P_{\mathrm{HB}}^{\mathrm{2nd}}$ is the second harmonic power allowed to circulate at a given frequency f_{fun}. It is important to highlight that f_{fun} does not represent necessarily the nominal output frequency but only the frequency at which the cell voltage ripple compensation is no longer needed, and the DAB can be disabled. As a result, the converter operates as a classical MMC.

III. SIMULATION RESULTS

Simulations are carried out in PLECS for a 10 SM per arm converter with the parameters of Table I. It is important to highlight that since the cell voltage is equal to V_{dc}/N, high switching frequencies can be achieved with inexpensive low-voltage, high-current silicon devices, enabling the converter to work with high fundamental frequencies.

A. Simulation Waveforms

In this section, simulation waveforms for the proposed topology are shown in order to validate the analytical analysis. Results are shown in Fig. 7. In Fig. 7(a) and (b), a fundamental frequency of 20 Hz is considered, and the DABs are disabled at $t = 0.2$. From the results it can be noted that when the DABs are disabled and, thus, the converter topology corresponds to a classical MMC, it is not possible to operate with the selected parameters. The SM capacitor voltages present a ripple superior to their nominal value, resulting in high distortion on the converter output. On the other hand, when the DABs are enabled, the converter operates with minimal output current distortions. Moreover, in Fig. 7(c), where the fundamental frequency is increased to 800 Hz, it can be noted that the DAB operation does not presents any particular advantage in terms of output currents

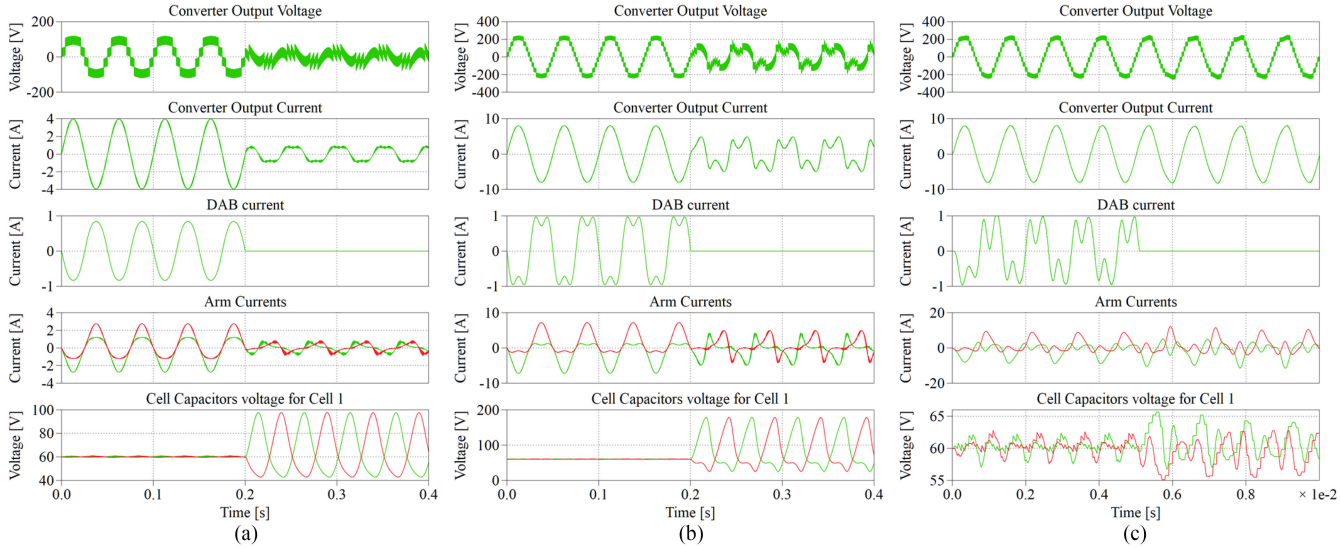


Fig. 7. Simulation results for: (a) fundamental frequency of 20 Hz and $m = 0.4$; (b) fundamental frequency of 20 Hz and $m = 0.8$; (c) fundamental frequency of 800 Hz and $m = 0.8$.

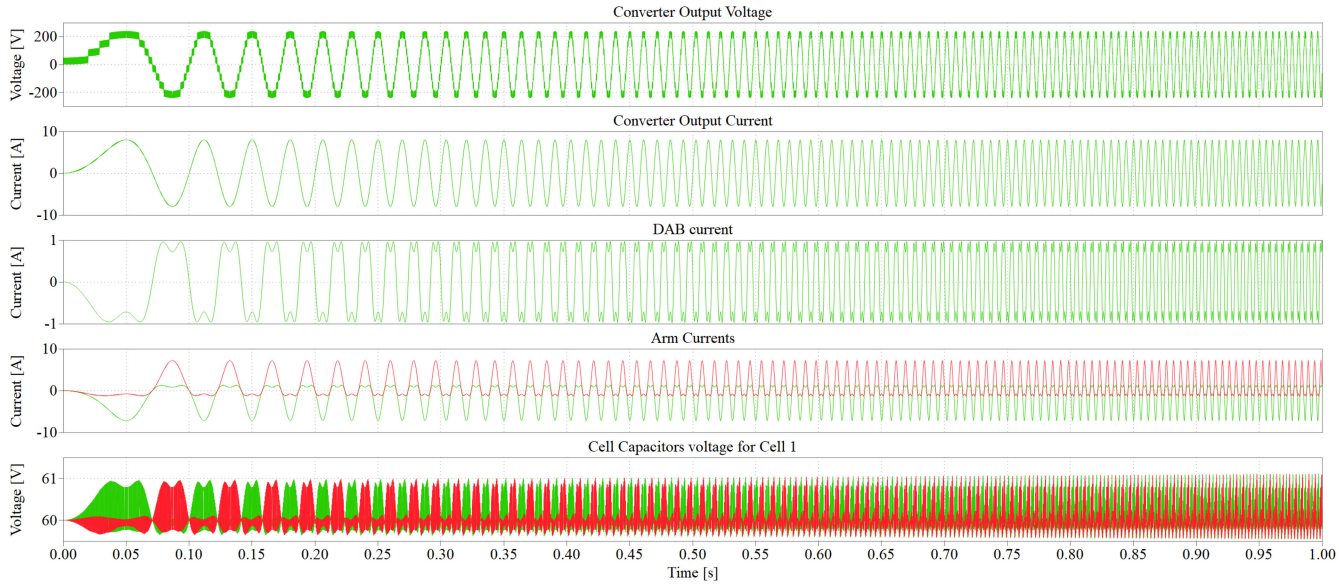


Fig. 8. Simulation results for a fundamental frequency sweep from 0 to 100 Hz with $m = 0.8$

distortions since the cell capacitance is high enough to passively absorb the voltage ripple at this fundamental frequency. Thus, the DAB can be disabled and the converter can be operated as a classical MMC, increasing the power conversion efficiency. In order to further corroborate the simulation results, Fig. 8 shows variable fundamental frequency converter operations, for 0–100 Hz. This scenario is very important, for example, in an automotive application where the electric drive is often required to operate at fundamental frequencies of few Hz, which are also critical for chain link converter topologies. From this figure, it is possible to notice that the converter is able to produce high-quality voltage and current waveforms in the whole fundamental frequency range under analysis. This is achieved by maintaining balanced SM capacitor voltages, which also presents a constant magnitude ripple. Finally, from the DAB current, it can be noted that the power managed by the DAB is maintained constant over the frequency range.

B. Simulations to Assess Converter Feasibility

In this section, an estimation of losses and THD for the proposed topology is performed and compared with a state of the art, two-level inverter based on a SiC power module. In order to perform this comparison, the converter load parameters are kept equal for the two topologies, considering a maximum output power of 15 kW. The SiC two-level inverter operates at a switching frequency of 100 kHz, which allows the converter to produce high-quality waveforms with the high fundamental frequency (up to 1 kHz in the considered design). The H-bridge switching frequency has been set to 10 kHz in order to produce

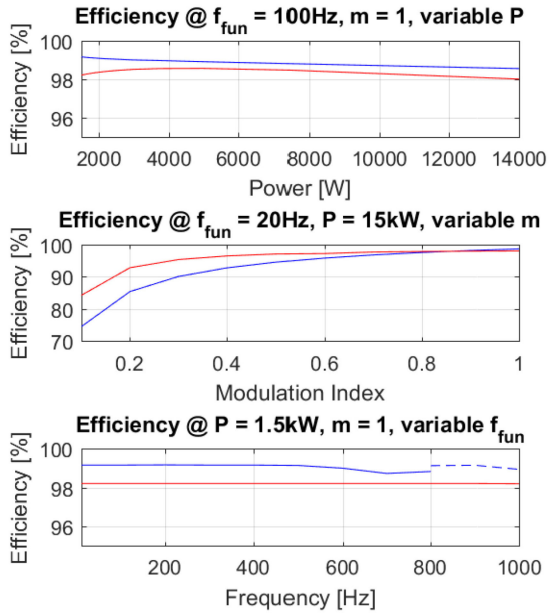


Fig. 9. Estimated converter efficiency in various operating conditions. Proposed topology (blue), proposed topology when DABs are disabled (dashed blue), SiC two-level inverter (red).

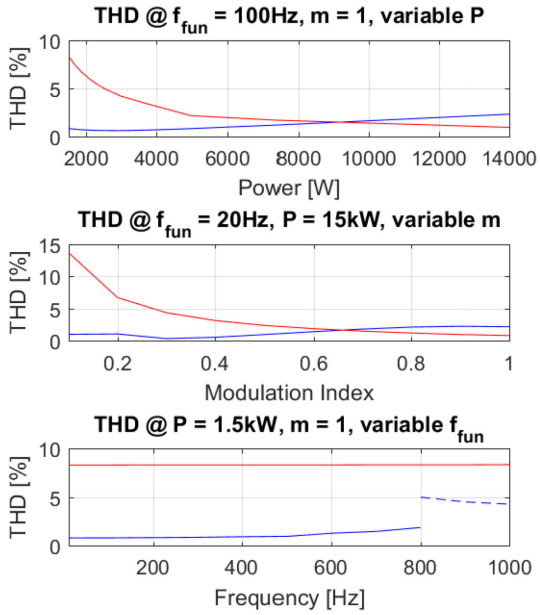


Fig. 10. Estimated converter THD in various operating conditions. Proposed topology (blue), proposed topology when DABs are disabled (dashed blue), SiC two-level inverter (red).

the same value of output switching frequency of the two-level inverter (100 kHz) when a 10 SM per arm topology is considered. The DABs switching frequency has been set to 100 kHz, in order to allow ripple power transfer from upper to lower arm and vice versa, with frequency up to three times the fundamental frequency (3 kHz in the considered design).

A qualitative analysis of losses is presented in Fig. 9, where only semiconductor losses are taken into account, considering Infineon IPT015N10N5 100 V, 300 A MOSFETs for the proposed topology and a Wolfspeed, 1.2 kV, 50A SiC Power Module (CCS050M12CM2) for the two-level inverter. The SiC power module has been chosen in order to maintain a high efficiency of the two-level inverter when the switching frequency is kept at 100 kHz. It is important to highlight that, considering the design power of 15 kW, this is hardly feasible with standard Si IGBT power modules. On the other hand, the MOSFET considered for the proposed topology has been selected considering a higher maximum current, in order to maintain comparable conduction losses between the proposed converter which presents $R_{\mathrm{DS,ON}}$ of 1.5 mΩ per device and the two-level inverter that presents an $\mathrm{R_{DS,ON}}$ of 25 mΩ per device. Moreover, this MOSFET is able to efficiently switch at 100 kHZ, which makes it suitable for use in the DAB converters. Using this design, all the considered devices present a dc voltage of approximately half of their maximum voltage, creating the conditions for a fair comparison between the converters.

Finally, since the analysis does not take into account passive components losses, it only provides a qualitative comparison between the converter operations and not represents a final value for the efficiency. An efficiency estimation at the variable fundamental frequency is provided in Fig. 9, showing a small impact on the efficiency value. However, it can be noted that at $f_{\mathrm{fun}} = 800$ Hz, the DABs in the proposed topology are disabled, increasing the efficiency at higher fundamental frequencies. The result in Fig. 9 shows that the proposed topology is able to operate with efficiency over 98% over a wide range of power, outperforming the SiC two-level inverter. On the other hand, the proposed topology presents low efficiency at low modulation indexes, as expected from the high number of switching devices present in this topology, and the SiC two-level is able to provide better results at modulation index up to 0.8.

A similar analysis is performed in order to compare the load current THD in several operating conditions. The results in Fig. 10 shows lower THD values for the proposed topology, with respect to the SiC two-level Inverter, with marginally higher THD values at higher power for the proposed topology. This effect is related to the residual voltage ripple harmonics on the capacitor voltages.

IV. Experimental Results

Preliminary experimental results are carried out on a 1 SM per arm prototype, shown in Fig. 11. The dc-link voltage and load parameters are scaled in order to match the waveforms of the simulation results presented in the previous section. In particular, a dc-link voltage of 60 V and a 30-Ω load with a 4.5-mH filter inductor are considered in the experimental setup.

The tests have been performed considering a custom-made Standex HF planar transformer. It is important to highlight that this configuration does not represent the final converter design that has been used only to validate the analysis performed in Section II and the simulation results in Section III-A.

Fig. 12 shows the converter waveforms when operating at 25, 50, and 100 Hz fundamental frequency, respectively. It can be noted that at 25-Hz fundamental frequency, the DAB has to be enabled in order to produce the desired output current,

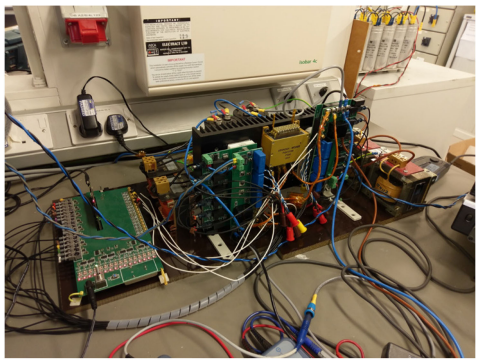
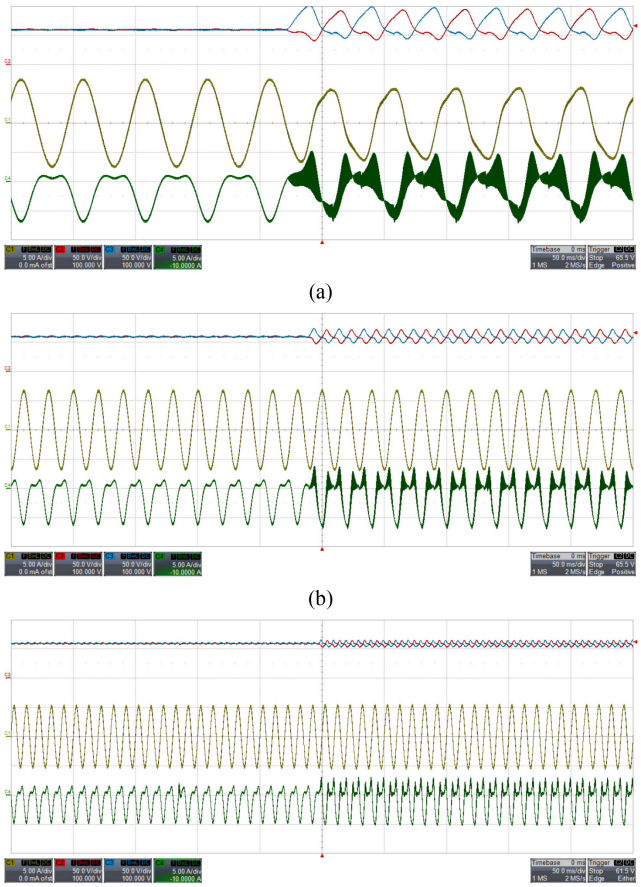


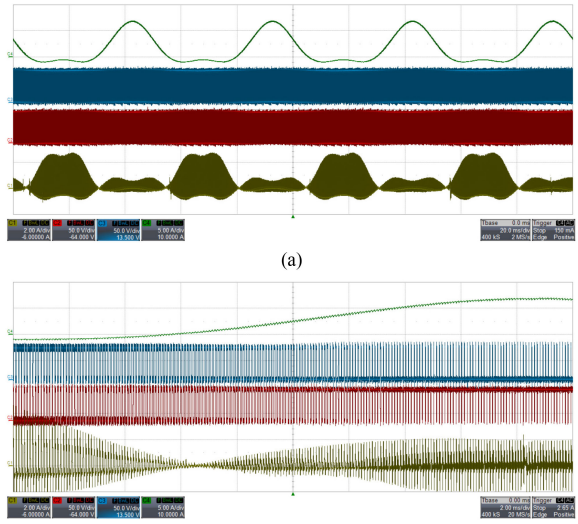
Fig. 11. Experimental prototype.



(a) (b) (c)

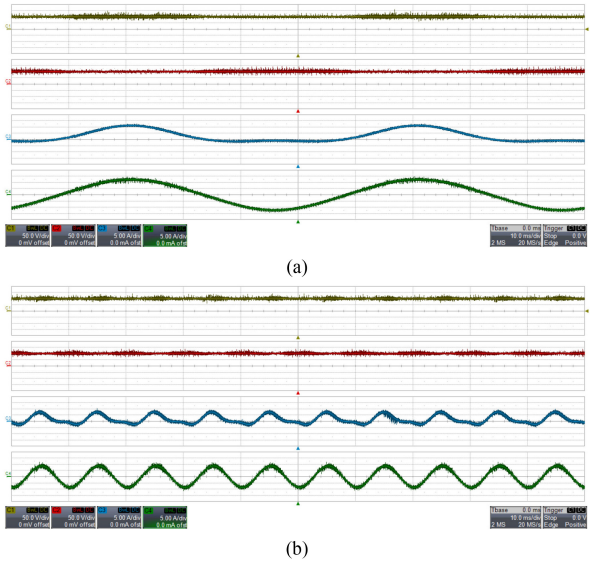
Fig. 12. Experimental waveforms for $m = 0.8$ and a fundamental frequency of (a) 25 Hz (b) 50 Hz (c) 100 Hz, 50 ms/div; i_{load} (yellow, 5 A/div), ${v_{\mathrm{c1}}}^{(u)}$ (red 50 V/div), ${v_{\mathrm{c1}}}^{(d)}$ (blue 50 V/div), ${i_{\mathrm{arm}}}^{(u)}$ (green 5 A/div).

thus validating the results obtained in the simulations. However, when the fundamental frequency is increased to 100 Hz, the cell capacitance is high enough to operate with a negligible SM capacitor voltage ripple even when the DAB is disabled. Fig. 13 shows the DAB waveforms validating the operation of the DAB converter. In particular, the switching current flowing through the DAB converter is highlighted showing that the DAB presents operation at a variable phase shift, in order to produce the desired power transfer through the two HB in the SM. Fig. 14 provides



(a) (b)

Fig. 13. Experimental waveforms for $m = 0.8$ and a fundamental frequency of 20 Hz (a) 20 ms/div and (b) 2 ms/div; switching DAB current i (yellow, 5 A/div), v_p (red 50 V/div), v_s(blue 50 V/div), ${i_{\mathrm{arm}}}^{(d)}$ (green 5A/div).



(a) (b)

Fig. 14. Experimental waveforms for $m = 0.8$ and a fundamental frequency of (a) 20 Hz, (b) 100 Hz, 10 ms/div; i_{load} (green, 5 A/div), ${v_{\mathrm{c1}}}^{(u)}$ (yellow 50 V/div), ${v_{\mathrm{c1}}}^{(d)}$ (red 50 V/div), ${i_{\mathrm{arm}}}^{(d)}$ (blue 5 A/div).

higher power results, with approximately 500 W managed by the SM, which corresponds to a 15-kW inverter where the configuration described in the Section III is considered. Results show good waveform quality and SM voltage stability at higher power, thus validating the feasibility of the proposed topology.

V. Conclusion

In this article, a novel chain-link topology, applicable to variable speed low-voltage drives, has been proposed. The topology features DAB power ripple interfaces between upper and lower arm HB modules. The topology analytical model has been derived, showing that it is possible to obtain the desired power transfer between the upper and lower arm without the

necessity of a closed-loop DAB control. Additionally, design guidelines for the proposed topology have been specified in this article. The derived models are validated through simulation and experimental testing and operation at different values of output power, fundamental frequency and modulation index are shown, highlighting the possibility of completely disabling the DAB operation over a certain value of fundamental frequency, which is related to the cell capacitance design. Moreover, a qualitative comparison of simulation results, in terms of device losses and output current THD, has been carried out. The comparison includes a two-level SiC inverter, operating with a switching frequency 10 times higher than the one of the proposed topology and the same load parameters. The results highlight the feasibility of such topology and the benefits it can provide in terms of design flexibility, losses management, and waveform quality. In conclusion, the proposed topology is able to maintain high output switching frequency and, thus, control of higher fundamental frequencies, without the need of using WBG devices. These features may result in reduced converter cost and EMI filtering requirements, whilst using well know and reliable Silicon devices. Moreover, its inherent modular structure could lead to an improved cooling system, due to the distribution of the power losses over several SMs and fault-tolerant capabilities, where the single SMs can be bypassed in case of fault, without interrupting the drive operations. These aspects will be the object of future studies.

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